**SFSU - ENGR 301 – ELECTRONICS LAB**

# LAB #5: MOSFET CHARACTERISTICS AND APPLICATIONS

Updated Dec. 30, 2003

## Objective:

To characterize *n-channel* and *p-channel enhancement MOSFETs*. To investigate basic *MOSFET amplifiers*. To compare *measured* and *simulated* MOSFET circuits.

## Components:

1 × CD4007UB MOSFET Arrays, 2 × 0.1 μF capacitors, 1 × 100 μF capacitor, 1 × 10 kΩ potentiometer, and resistors: 1 × 100 Ω, 2 × 10 kΩ, and 1 × 1 MΩ (all 5%, ¼ W).

## Instrumentation:

A bench power supply, a waveform generator (sine/triangle wave), a digital multi-meter, and a dual-trace oscilloscope.

## PART I – THEORETICAL BACKGROUND

Figure 1 shows the circuit symbols for the *n-channel* and the *p-channel enhancement* MOSFETS, the devices we are going to be using in this lab. The *gate* (*G*) of the MOSFET plays a similar role to the base (*B*) of the BJT. Similarly, the *drain* (*D*) can be likened to the collector (*C*), and the *source* (*S*) to the emitter (*E*). As in the case of BJTs, the *current directions* and *voltage polarities* of one device are *opposite* to those of the other. In fact, the *n*- and the *p*-channel devices are said to be *complementary* to each other, and when they are fabricated on the same substrate, the resulting technology is referred to as *complementary MOS*, or CMOS for short. Unlike the BJT, which requires a base current to go on, the FET has $i_G = 0$. Consequently, for FETs we have $i_S = i_D$.

MOSFETs possess a fourth terminal called the *body* (*B*), which is internally tied to the *substrate*. Though this terminal is not used on purpose, it must be properly biased to prevent unintentional effects. In the *n*-channel MOSFET the body forms a *pn* junction both with the source and the drain regions, with *B* acting as the *anode*. To avoid inadvertently turning on either of these junctions, we must at all times hold *B* at the *most negative voltage* (MNV). Likewise, in the *p*-channel MOSFET, *B* acts as the *cathode*, so it must be held at the *most positive voltage* (MPV). When physically possible, *B* is tied to *S*, and the above constraints are satisfied automatically. This will be the case with the devices of this lab.

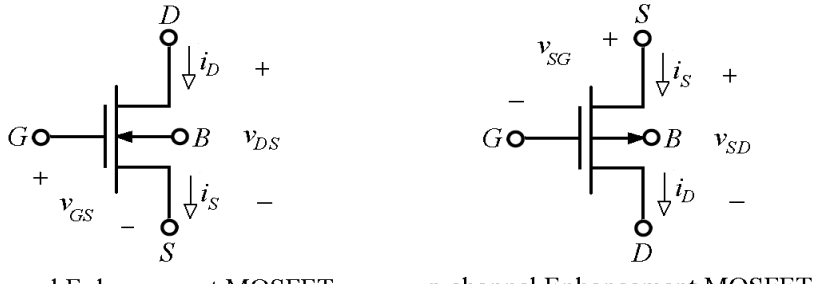



**Fig. 1** – Circuit symbols, current directions, and voltage polarities for the MOSFETs.

When an *n*-channel MOSFET (*n*MOSFET*)* is biased in the *pinchoff region*, also called *saturation region* or *active region*, and characterized by the conditions

$$v_{GS} \geq V_{tn} \tag{1a}$$

$$v_{DS} \geq v_{GS} - V_{tn} \tag{1b}$$

its *drain current* $i_D$ depends on the applied *gate-source* voltage $v_{GS}$ and the operating *drain-source* voltage $v_{DS}$ as

$$i_D = \frac{k_n}{2}\left(v_{GS} - V_{tn}\right)^2\left(1 + \lambda_n v_{DS}\right) \tag{2}$$

where

- $k_n$ is a scale factor known as the *device transconductance parameter*, in $A/V^2$
- $V_{tn}$, known as the *threshold voltage*, is the value of $v_{GS}$ at which the MOSFET starts conducting
- $\lambda_n$, whose dimensions are $V^{-1}$, is called the *channel-length modulation parameter* ($\lambda_n$ is the reciprocal of the *Early voltage* $V_{An}$ of an *npn* BJT, or $\lambda_n = 1/V_{An}$).

For a low-power *n*MOSFET, $k_n$ is typically in the range of $10^2$ $\mu A/V^2$, $V_{tn}$ is in the range of $10^0$ V, and $\lambda_n$ is on the order of $10^{-2}$ $V^{-1}$. If $V_{tn} > 0$, the *n*MOSFET is said to be of the *enhancement type*; if $V_{tn} < 0$, it is said to be of the *depletion type*. Moreover, the extrapolated value of $i_D$ in the limit $v_{DS} \to 0$ is $i_D = (k_n/2)(v_{GS} - V_{tn})^2$.

The *device transconductance parameter* $k_n$ depends on device geometry as

$$k_n = k_n'\left(\frac{W_n}{L_n}\right) \tag{3}$$

where

- $k_n'$, also in $A/V^2$, is called the *process transconductance parameter*;
- $W_n$ and $L_n$, both in μm, are the channel *width* and channel *length* of the *n*MOSFET

Similar considerations hold for the *p*-channel MOSFET (*p*MOSFET), provided we *reverse* all *current directions* and *voltage polarities*. Thus, the active-region conditions of Eq. (1) become, for a *p*MOSFET,

$$v_{SG} \geq -V_{tp} \tag{4a}$$

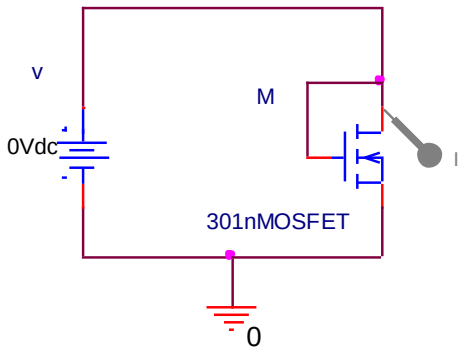
$$v_{SD} \geq v_{SG} + V_{tp} \tag{4b}$$

Similarly, Eq. (2) is rephrased as

$$i_D = \frac{k_p}{2}\left(v_{SG} + V_{tp}\right)^2\left(1 + \lambda_p v_{SD}\right) \tag{5}$$

where

$$k_p = k_p'\frac{W_p}{L_p} \tag{6}$$




$W_n = 10\ \mu m$
$L_n = 5\ \mu m$
$k' = 50\ \mu A/V^2$
$V_{tn} = 1.5\ V$
$\lambda_n = 0.05\ V^{-1}$

**Fig. 2** – PSpice circuit to plot the *i-v* characteristic of a homebrew *n*MOSFET operated in the so called *diode mode* (*G* and *D* tied together, and *B* and *S* tied together. ).

is again the *device transconductance* parameter, and $k_p'$ the *process transconductance* parameter, both in $A/V^2$. , and If $V_{tp} < 0$, the *p*MOSFET is said to be of the *enhancement type*; if $V_{tp} > 0$, it is said to be of the *depletion type*. The extrapolated value of $i_D$ in the limit $v_{SD} \to 0$ is $i_D = (k_p/2)(v_{SG} + V_{tp})^2$.

MOSFET circuits are readily simulated via PSpice. In the PSpice circuit of Fig. 2 we are using a homebrew *n*MOSFET called 301nFET to display the $i_D$ versus $v_{GS}$ characteristic in the so called *diode mode* of operation (*G* and *D* tied together). This device has been created by renaming and suitably editing the *PSpice Model* of one of the MOSFETs available in the PSpice Library. This has been done first by clicking the device to select it, then by clicking **Edit → PSpice Model** to change the values of its parameters. The result is the following model statement:

```
.model 301nMOSFET        NMOS(W=10u L=5u kp=50u Vto=1.5 lambda=0.05)
```

The characteristic, expressed by Eq. (2) and shown in Fig. 3, is reminiscent of a diode curve.

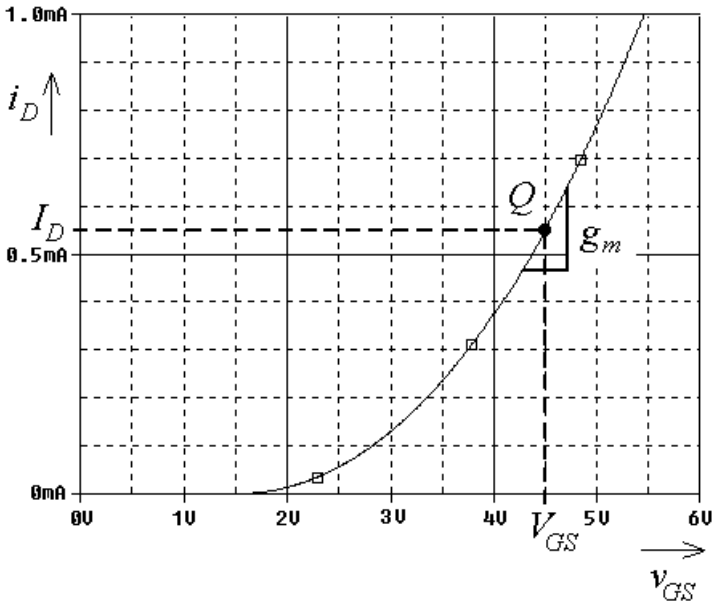



**Fig. 3** – The *i-v* characteristic of the diode-connected *n*MOSFET of Fig. 2.

The slope of the $i_D$ –$v_{GS}$ curve at a particular *operating point* $Q(I_D, V_{GS})$ is denoted as $g_m$, and is called the *transconductance*, in A/V or also in 1/Ω. (Beware not to confuse $g_m$ with $k$ or $k'$, whose units are $A/V^2$) Upon differentiating Eq. (2), we end up with three expressions,

$$g_m = k_n(V_{GS} - V_{tn}) = \sqrt{2k_n I_D} = \frac{I_D}{0.5(V_{GS} - V_{tn})} \tag{7}$$

Likewise, a *p*MOSFET has $g_m = k_p(V_{GS} + V_{tp}) = \sqrt{2k_p I_D}$ . Compared to a BJT, for which $g_m = I_C/V_T = I_C/(26\text{ mV})$, an *n*MOSFET has $g_m = I_D/[0.5(V_{GS} - V_{tn})]$, where usually $0.5(V_{GS} - V_{tn}) >> 26$ mV. This explains why MOSFETs in general have notoriously *much lower* $g_m$s than their BJT counterparts. Indeed, our homebrew *n*MOSFET, whose $k_n$ is typical of small-geometry devices, has $g_m(I_D = 1\text{ mA}) = 0.632$ mA/V = 1/(1580 Ω). Conversely, a BJT has $g_m(I_C = 1\text{ mA}) = 38$ mA/V = 1/(26 Ω).

It is interesting to note that if we plot the *i*-*v* characteristic of a diode-connected MOSFET on a *quadratic*-versus-*linear* system of axes, the resulting curve becomes a *straight line*. Specifically, if we plot Eq. (2) on an *x*-*y* plane with

$$x = v_{GS} \; (= v_{DS}) \tag{8a}$$

and

$$y = \sqrt{\frac{i_D}{1 + \lambda_n x}} \tag{8b}$$

then the characteristic becomes $y = \sqrt{k_n/2}(x - V_{tn})$ , that is, a straight line with *slope* $dy/dx = \sqrt{k_n/2}$ and *x*-axis *intercept* at $V_{tn}$. This is illustrated in Fig. 4 for our homebrew *n*MOSFET. We shall find this feature quite convenient from an experimental standpoint.

An insightful alternative for illustrating *n*MOSFET operation is by plotting $i_D$ versus $v_{DS}$ for different values of $v_{GS}$. The PSpice circuit of Fig. 5 generates such a plot for incremental steps in $V_{GS}$ of 0.5 V each. The resulting family of curves, shown in Fig. 6, reveals *three regions* of operation:

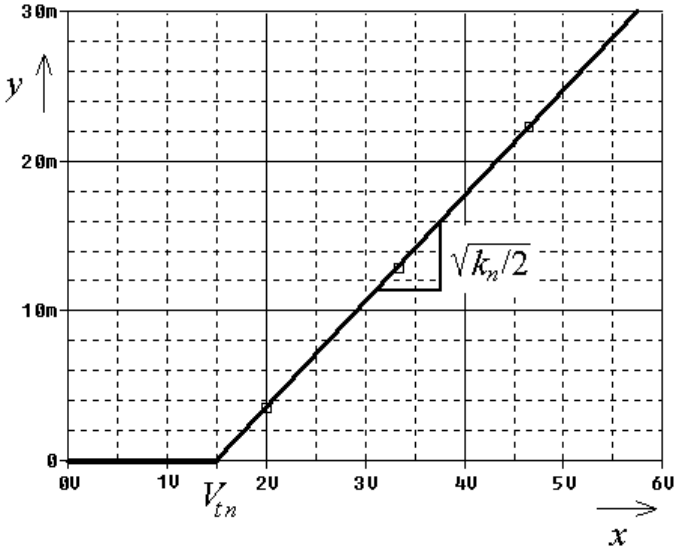



**Fig. 4** – Linearization of the *i*-*v* curve of a diode-connected *n*MOSFET.

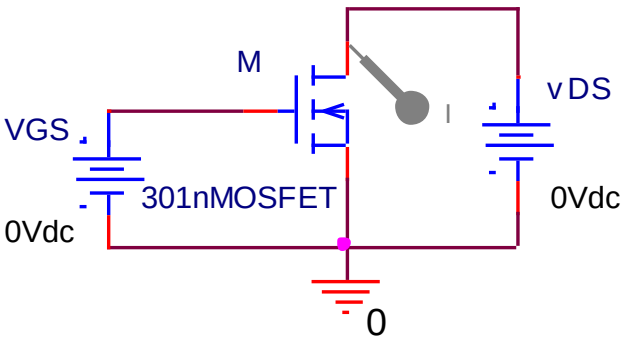



**Fig. 5** - PSpice circuit to plot $i_D$ versus $v_{DS}$ for different values of $V_{GS}$.

- For $v_{GS} \le V_{tn}$ (= 1.5 V) we get $i_D = 0$, indicating that the *n*MOSFET is operating in the ***cutoff* (CO) *region***. In this region both the *GS* and *DS* ports act as *open circuits*.
- For $v_{GS} > V_{tn}$, the *n*MOSFET is *on*. The region corresponding to $v_{DS} > V_{GS} - V_{tn}$ is called the ***pinchoff*** (PO), or ***saturation***, or ***active*** region. As we know, in this region Eq. (2) holds, which we repeat here

$$i_D = \frac{k_n}{2}\left(v_{GS} - V_{tn}\right)^2\left(1 + \lambda_n v_{DS}\right) \qquad \text{for } v_{DS} > V_{GS} - V_{tn} \qquad (9)$$

In the PO region, the $i_D$ versus $v_{DS}$ curves are almost *horizontal*, indicating *current-source* behavior by the *DS* port there. Moreover, if we project the PO curves to the left, they all converge to the *same point* on the $v_{DS}$ axis. This point is located at $-1/\lambda_n$V. Note that when operated in the diode mode, the MOSFET has $v_{DS} = v_{GS}$, which obviously satisfies $v_{DS} > V_{GS} - V_{tn}$, indicating PO operation when the device is on.

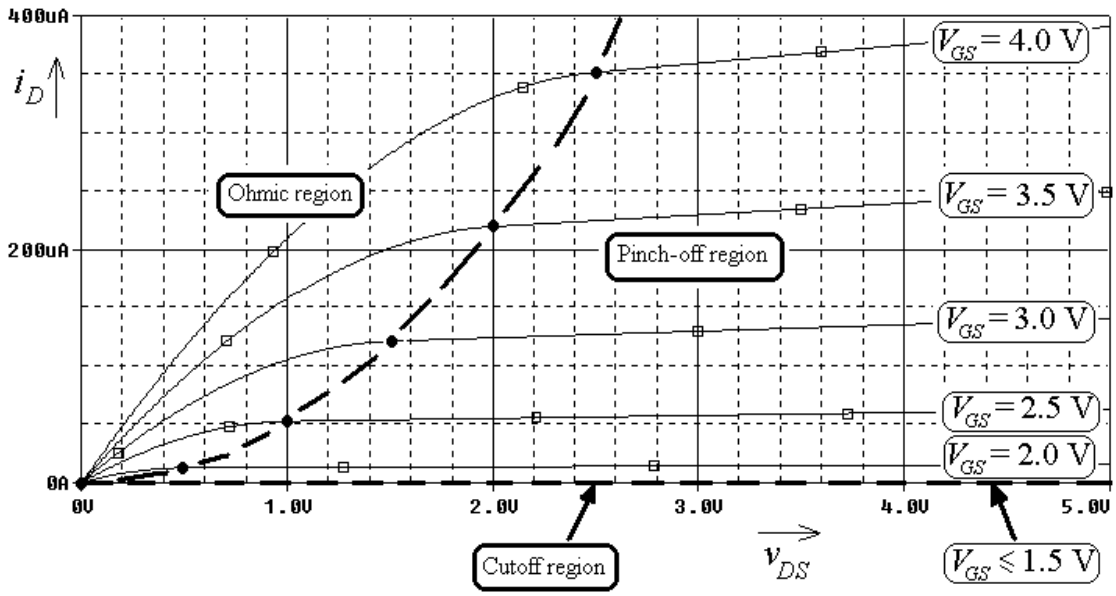



**Fig. 6** – Illustrating the *three* regions of operation of an *n*MOSFET.

- The region corresponding to $v_{DS} < V_{GS} - V_t$ is called the ***ohmic*** (Ω), or ***triode*** region. In this region the channel behaves as a nonlinear resistor, and $i_D$ takes on the form

$$i_D = k_n\left[\left(v_{GS} - V_{tn}\right)v_{DS} - \frac{{v_{DS}}^2}{2}\right]\left(1 + \lambda_n v_{DS}\right) \qquad \text{for } v_{DS} < V_{GS} - V_{tn} \tag{10}$$

For small values of $v_{DS}$, we can ignore $v_{DS}^2/2$ as well as $\lambda_n v_{DS}$ (recall that $\lambda_n << 1$), and approximate

$$i_D \cong \frac{1}{r_{DS}} v_{DS} \tag{11a}$$

where

$$r_{DS} = \frac{1}{k_n(V_{GS} - V_{tn})} \tag{11b}$$

represents the *channel resistance* in the limit $v_{DS} \to 0$. Such a resistance is controlled by $V_{GS}$, indicating *voltage-controlled resistance* behavior near the origin. As shown in Fig. 6, the borderline between the PO and the Ω regions is a locus of points forming a *parabola*.

As we know, it is convenient to express a *total signal* such as the drain current $i_D$ as the sum

$$i_D = I_D + i_d \tag{12}$$

where

- $I_D$ is the *DC component*, also known as *large signal*
- $i_d$ is the *AC component*, also known as *small signal*

We work with DC signals when dealing with transistor *biasing*, and we work with AC signals when dealing with *amplification* to find AC *gain* as well as in *input* and *output resistances*. To signify how a FET relates DC voltages and currents (upper-case symbols with upper-case subscripts) we use *large signal models*, while to signify how it relates AC voltages and currents (lower-case symbols with lower-case subscripts) we use the *small-signal model*.

## Large-Signal MOSFET Models:

With regard to the two regions of interest to us in this laboratory, namely the CO and the PO regions, we make the following observations:

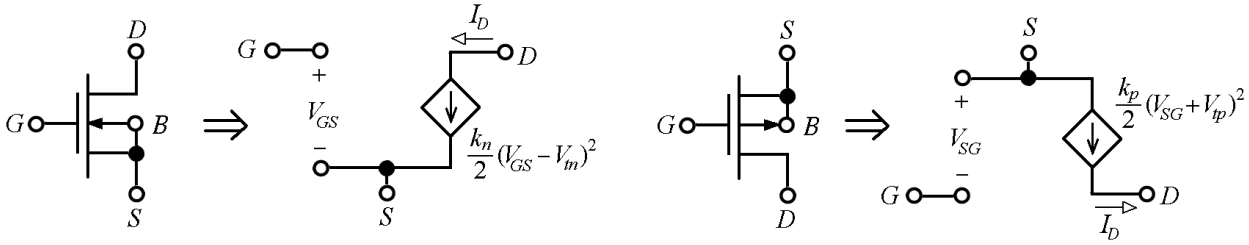



**Fig. 7** – Large-signal MOSFET models

In the *CO region* a MOSFET draws only leakage currents, which for practical purposes can be neglected. So, both the *GS* and the *DS* ports act essentially as *open circuits*.

- In the *PO region*, the *GS* port still acts as an open circuit, but the *DS* port now acts as a *dependent current source*, which in the case of the *n*MOSFET takes on the form $I_D \cong (k_n/2)(V_{GS} - V_{tn})^2$, where we are arbitrarily assuming $\lambda_n = 0$ to simplify our DC calculations. Similar considerations hold for the *p*MOSFET, and the two models are shown in Fig. 7.

**Small-Signal MOSFET Model:**

When used as an *amplifier*, a MOSFET is operated in the *PO region* where we model its way of relating voltage and current *variations* via the *small signal model*. Due to its quadratic characteristic, the BJT is a nonlinear device. However, if we stipulate to keep its *signal variations sufficiently small* (hence the designation *small-signal*), then the model can be kept linear – albeit approximate. For an *n*MOSFET, the small signal constraint is

$$v_{gs} << 2(V_{GS} - V_{tn}) \tag{13}$$

while for a *p*MOSFET it is $v_{gs} << 2(V_{SG} + V_{tp})$. Note that the large-signal models are different for the two MOSFET types because their voltage polarities and current directions, are *opposite*. However, the small-signal model is the *same* for the two types because it involves only *variations*. This common model is shown in Fig. 8. Its parameters depend on the *bias current* $I_D$ as

$$g_m = \sqrt{2kI_D} \qquad\qquad r_o = \frac{1}{\lambda I_D} \tag{14}$$

At the same bias current, the $r_o$ of a MOSFET is typically on the same order of magnitude as that of a BJT. However, the $g_m$ of a MOSFET is typically one to two orders of magnitude *smaller*. This is due to the fact that the *i-v* characteristic of the MOSFET is *quadratic*, while that of the BJTis *exponential* and thus generally much steeper. For the same reason, the MOSFET is not as pronouncedly nonlinear as the BJT, so the small-signal constraint of Eq. (13) is generally far more relaxed than for a BJT, for which $v_{be}$ << 52 mV.

The relationships presented in Lab #4 for the generalized ac equivalent of the BJT hold also for the MOSFET, the only difference being that the MOSFET has $i_g = 0$ and generally much lower $g_m$ under

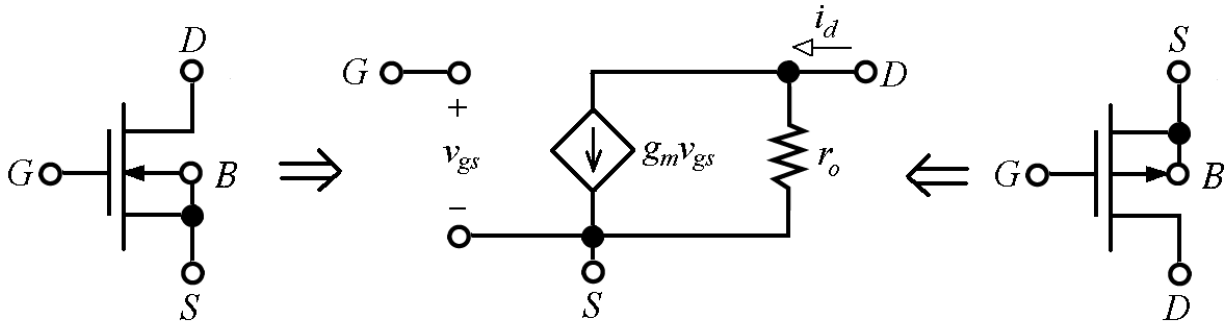



**Fig. 8** – Small-signal MOSFET model, valid for $v_{gs} << 2(V_{GS} - V_t)$.

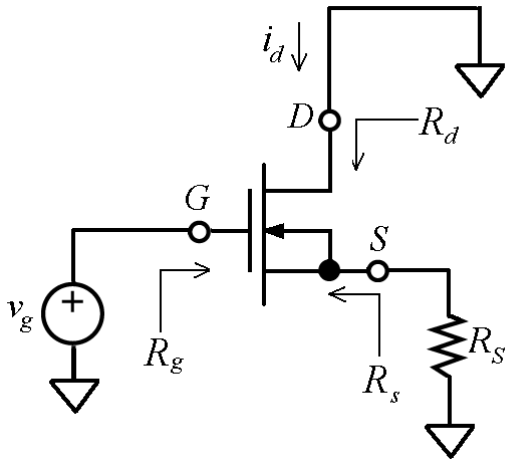



**Fig. 9** – Generalized AC equivalent.

similar operating conditions. With reference to Fig. 9, the relationships are as follows:

- The ***input resistance*** seen looking into the ***gate*** is

$$R_g = \infty \tag{15}$$

  indicating that we can bias the gate of a MOSFET with resistances in the MΩ range, if needed.

- The ***output resistance*** seen looking into the ***source*** is

$$R_s = \frac{1}{g_m} \tag{16}$$

  which is generally low, but not as low as in the case of a BJT operating under similar conditions. For a low-power MOSFET operating at $I_D$ = 1 mA, $R_s$ is typically in the kΩ range. As we know, a BJT has $r_e$(1 mA) = 26 Ω.

- The ***output resistance*** seen looking into the ***drain*** is

$$R_d = r_o\left(1 + g_m R_S\right) \tag{17}$$

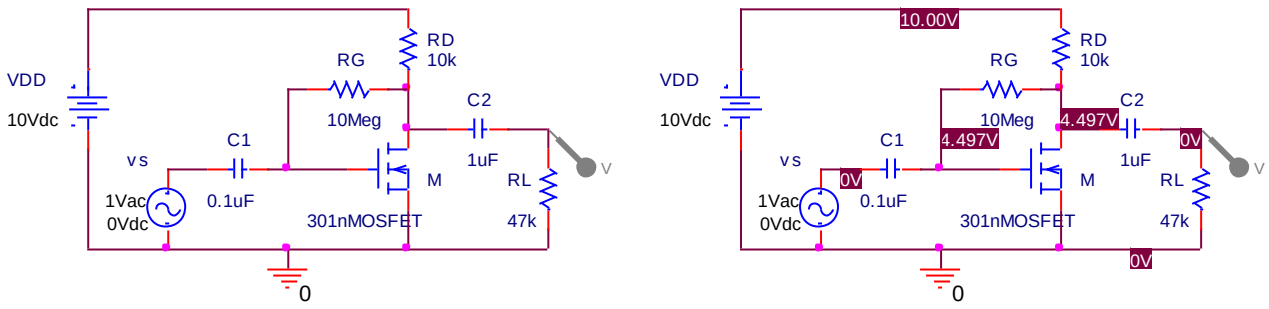
  indicating that the presence of $R_S$ effectively *raises* the drain resistance from $r_o$ to $R_d$.

- The change in drain current $i_d$ stemming from a small-signal change in the gate voltage $v_g$ is expressed as $i_d = G_m v_g$, and we have

$$G_m = \frac{g_m}{1 + g_m R_S} \tag{18}$$

  indicating that the presence of the source resistance $R_S$ introduces *source degeneration*.

We conclude by illustrating the use of PSpice to simulate a *common-source* (CS) *amplifier*. You can simulate this circuit on your own by downloading its appropriate files from the Web. To this end, go to http://online.sfsu.edu/~sfranco/CoursesAndLabs/Labs/301Labs.html, and once there, click on **PSpice Examples**. Then, follow the instructions contained in the **Readme** file. Our PSpice circuit is shown in Fig. 10*a*. After directing PSpice to perform the *Bias Point Analysis*, we obtain the




(*a*) (*b*)

**Fig. 10** – Common-source amplifier and its DC voltages

labeled schematic of Fig. 10*b*. Moreover, after directing PSpice to perform a one-point *AC Analysis* at $f$ = 10 kHz, we find that the *small-signal gain* of the circuit is $A_v = v_o/v_i = -2.55$ V/V. You will find it quite instructive to confirm the above data (both bias and AC) via hand calculations!

## Part II – Experimental Part

We shall perform our experiments using the CD4007UB MOSFET Array. This array consists of three *n*MOSFETs and three *p*MOSFETs, all of the enhancement type, interconnected in the manner depicted in Fig. 11. Recall that the body of the *n*MOSFETs (pin 7) must always be held at the *most negative voltage* (MNV) in the circuit; while the body of the *p*MOSFETs (pin 14) must always be held at the *most positive voltage* (MPV) in the circuit. Failure to respect these constraints may invalidate all measurements taken.

The CD4007 is a delicate device. To avoid damaging it, make sure that you always *turn power off* before making any circuit changes, and that before reapplying power, each lab partner performs a *separate check* that the circuit has been wired correctly. Also, refer to the Appendix for useful tips on

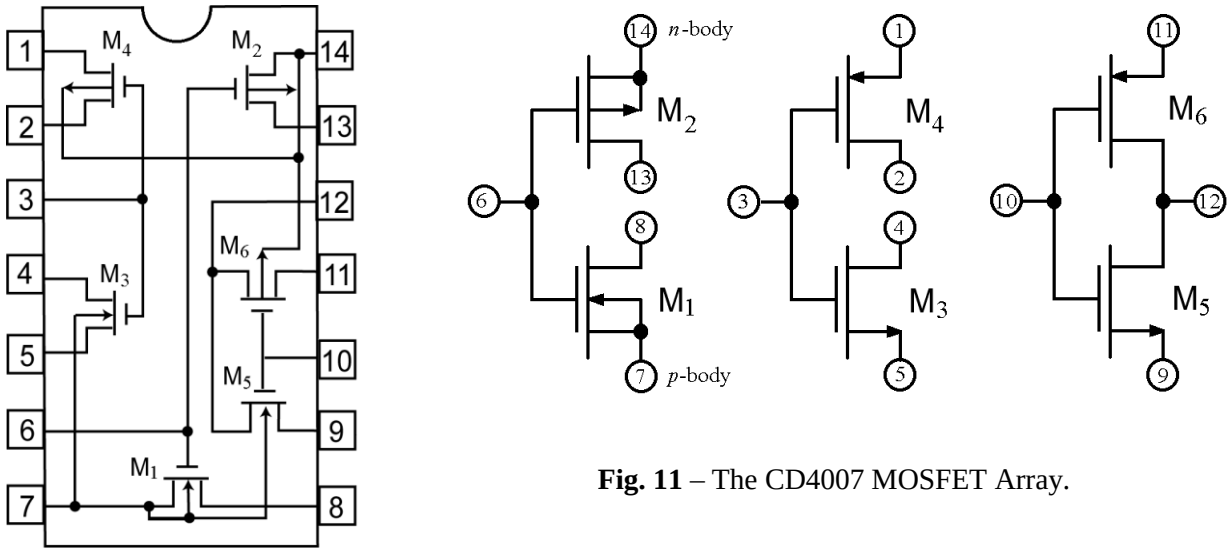



**Fig. 11** – The CD4007 MOSFET Array.

how to wire proto-board circuits. The hand calculations and PSpice simulations that you will perform in this and the following lab rely on the measurements taken for a *particular CD4007 sample*, so if you are careless and end up damaging it, you'll have to perform each measurement all over again!

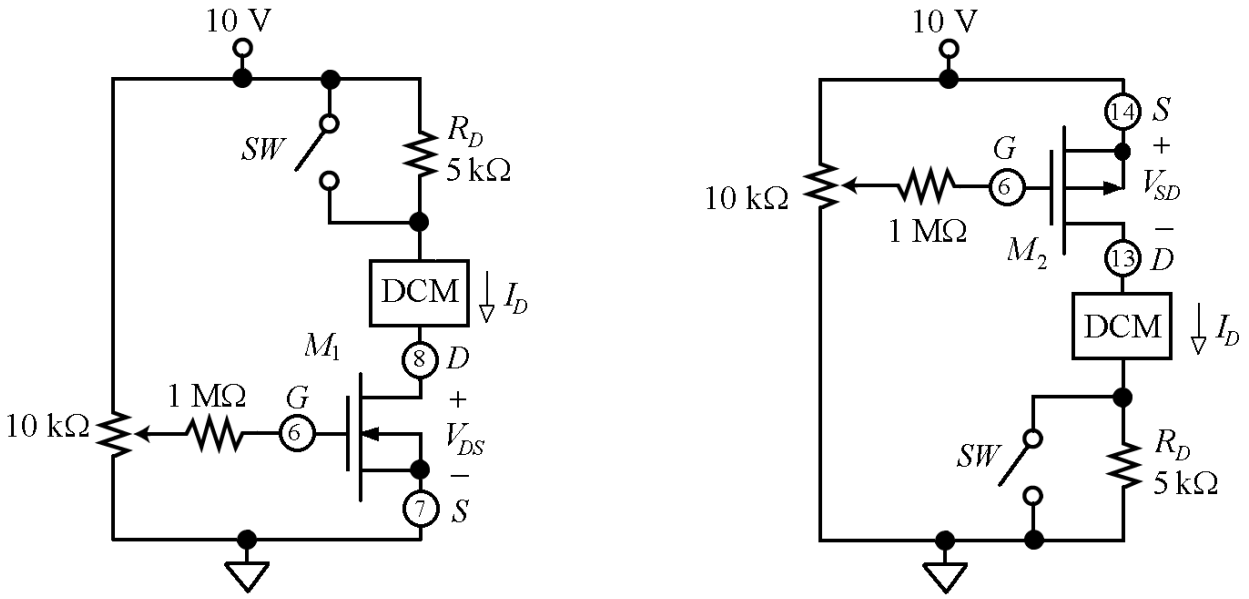
You are urged to compare the data you are measuring on your *particular* sample against those reported in the data sheets, which are *typical* in that they were obtained by averaging over a large number of samples. To download the data sheets from the Web, go to http://www.google.com and search for "CD4007UB" or variants thereof.

## MOSFET Characterization:

**MC1:** We use the circuits of Fig. 12 to find $\lambda_n$ and $\lambda_p$. Mark one of the CD4007 ICs (the other is a spare). Turning first to the *n*MOSFET, assemble the circuit of Fig. 12*a* with power off (for $R_D$ use 2 × 10 kΩ resistors in parallel). Using your multi-meter as a *digital current meter* (DCM), insert it in series between $R_D$ and the drain *D*, as shown. Apply power and adjust the potentiometer for $I_D$ = 1 mA. With reference to Fig. 13, this will bias $M_1$ at the operating point $Q(I_D , V_{DS}) = Q(1\text{ mA}, 5\text{ V})$. Now short out $R_D$ with a wire (that is, close *SW*) to change the operating point from *Q* to *Q*' with $\Delta V_{DS}$ = 5 V, and then measure the corresponding change $\Delta I_D$. Expect the latter to be small, so use as many digits as your ammeter will allow. Finally, find $r_o = \Delta V_{DS}/\Delta I_D$ and $\lambda_n = 1/(r_o I_D - V_{DS})$. Are your values typical?

**MC2:** Repeat Step MC1 for the *p*MOSFET of Fig. 12*b*, except that you now find your parameters as $r_o = \Delta V_{SD}/\Delta I_D$, and $\lambda_p = 1/(r_o I_D - V_{SD})$. Again, are your values typical? How do their magnitudes compare with those of the *n*MOSFET of Step MC1?

**M3:** We use the circuits of Fig. 14 to find $k_n$ and $V_{tn}$, and $k_p$ and $V_{tp}$. Turning first to the *n*MOSFET, assemble the circuit of Fig. 14*a* with the DCM in series with the drain *D*. Obtain *v* from one of your variable power supplies, and measure and record *i* for *v* = 0 V, 1 V, 2 V, 3 V, 4 V, and 5 V.




(*a*) (*b*)

**Fig. 12** – Test circuits to find $\lambda_n$ and $\lambda_p$.

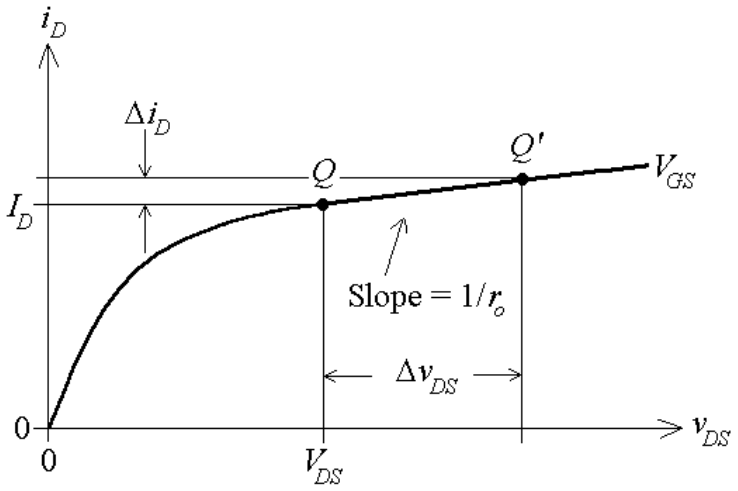
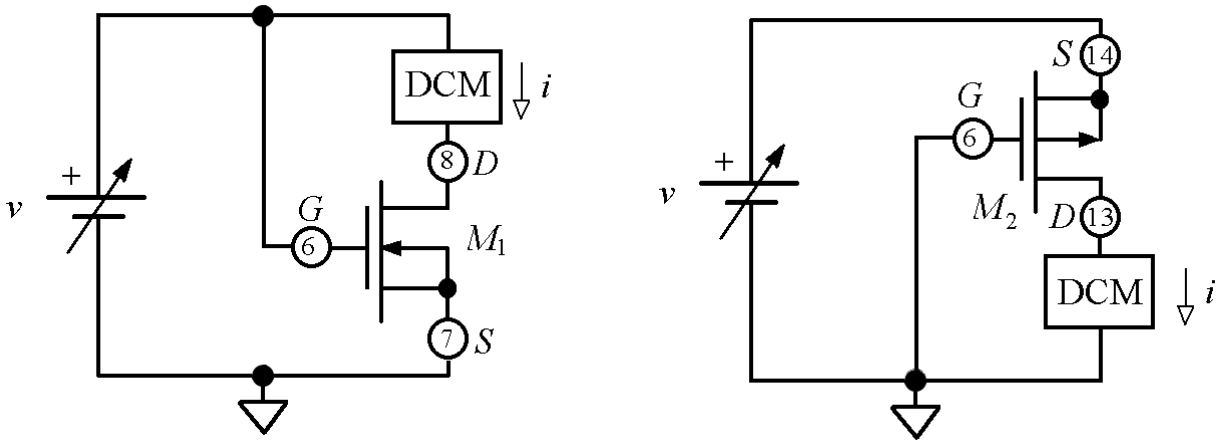



**Fig. 13** – Graphical illustration for finding $r_o$ and hence $\lambda_n$ and $\lambda_p$.

**C4:** Consider the data of Step M3 for which $i > 0$, and plot them on an $x$-$y$ graph, with $x = v$ and $y = \sqrt{i/(1+\lambda_n x)}$ (use the value of $\lambda_n$ found in Step MC1.) Hence, find the *best fit straight line*, determine its slope $dy/dx$, and obtain $k_n = 2(dy/dx)^2$. Moreover, obtain $V_{tn}$ as the value of $x$ where your line intercepts the $x$-axis. Are your values typical?

**M5:** Repeat Step M3 for the *p*MOSFET of Fig. 14*b*.

**C6:** Consider the data of Step M5 for which $i > 0$, and plot them on an $x$-$y$ graph, with $x = v$ and $y = \sqrt{i/(1+\lambda_p x)}$ (use the value of $\lambda_p$ found in Step MC2.) Hence, find the *best fit straight line*, determine its slope $dy/dx$, and obtain $k_p = 2(dy/dx)^2$. Moreover, obtain $V_{tp}$ as the *negative* of the value of $x$ where your line intercepts the $x$-axis. Are your values typical? How do they compare with those of the *n*MOSFET?




(*a*) (*b*)

**Fig. 14** – Test circuits to find $k_n$, $V_{tn}$, $k_p$, and $V_{tp}$.

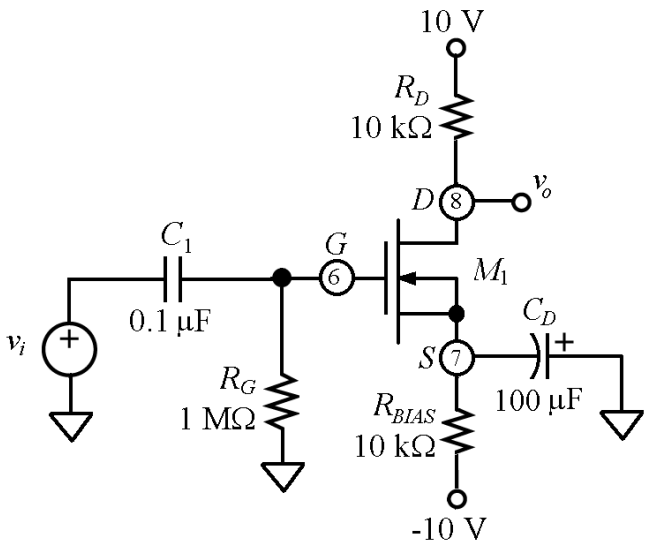



**Fig. 15** – *Common-source* (CS) amplifier.

## Common-Source Amplifier:

**C7:** Using the large-signal *n*MOSFET model with the parameters just measured, predict the DC voltages $V_G$, $V_D$, and $V_S$ at the gate, drain, and source terminals of the *common-source* amplifier of Fig. 15. Hence, find the DC drain current $I_D$, and predict the value of the small-signal gain $A_v = v_o/v_i$, which in this case is

$$A_v = -g_m(r_o // R_D) \tag{19}$$

with $g_m$ given in Eq. (14).

**M8:** With power off, assemble the circuit of Fig. 15, but without connecting the waveform generator yet. Apply power, and use your DVM to measure the DC voltages $V_G$, $V_D$, and $V_S$. Next, connect the waveform generator, and while monitoring $v_i$ with Ch.1 of the oscilloscope, adjust the generator so that $v_i$ is a 10-kHz *sine-wave* with 0-V DC and 1-V *peak-to-peak* amplitude. Finally, use Ch. 2 (set on AC) to measure the *peak-to-peak amplitude* of $v_o$, and then find the experimental gain $A_v = v_o/v_i$ of your amplifier.

**S9:** Simulate the circuit of Step M8 via PSpice (DC as well as AC analysis). For a realistic simulation you need to create a PSpice model for your specific *n*MOSFET sample, using the above-measured values of $k_n$, $V_{tn}$, and $\lambda_n$. To this end, when in PSpice, click the device to select it, then click **Edit → PSpice Model** to change the values of its parameters to those found experimentally.

***Note:*** From the above measurements you have no way to know the values of $W_n$ and $L_n$. What you can do is to arbitrarily assume $W_n = L_n$ (say, 5- μm each), and then set the model parameter "Kp" to the value you have found for $k_n$. By this simple trick, PSpice will end up using the correct value for $k_n$.

**C10:** Compare the *predicted* values of Step C7 with the *measured* ones of Step M8 and the *simulated* ones of Step S9. Account for possible discrepancies.

**M11:** Returning to the circuit of Fig. 15, switch Ch. 2 to the DC mode (make sure you know where your 0-V baseline is on the screen!), change the waveform generator from sine-wave to *triangle-wave*, and increase its amplitude until $v_o$ distorts both at the top and at the bottom. Justify the two types of distortion in terms of transistor operation.

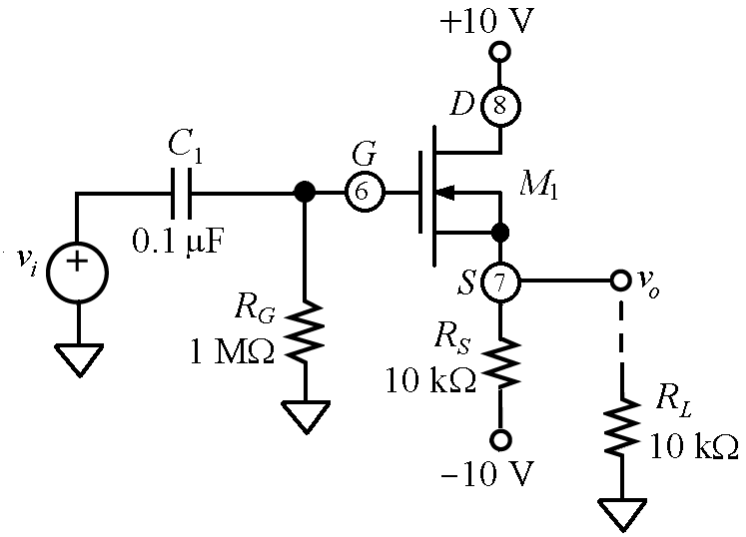



**Fig. 16** - *Common-drain* (CD) amplifier.

## Common-Drain Amplifier:

**C12:** Assuming $v_i$ has a DC value of 0 V in Fig. 16, use the large-signal model to find the DC drain current $I_D$. Hence, predict the value of the small-signal gain $A_v = v_o/v_s$, which in this case is

$$A_v = \frac{1}{1+\dfrac{1}{g_m(R_S \,//\, r_o)}} \tag{20}$$

Also, predict the value of the output resistance seen by the load, which in this case is $R_o = (1/g_m)//R_S$.

**M13:** With power off, assemble the circuit of Fig. 16 (don't connect $R_L$ yet.) Keep leads short, and mount the 0.1-μF power-supply bypass capacitors in *close proximity* to your IC. Next, apply power, adjust the waveform generator so that $v_i$ is a 10-kHz *sine-wave* with 0-V DC and a *peak-to-peak* amplitude of 2 V, and measure the gain $A_v = v_o/v_i$. How does it compare with the predicted value of Step C12? What happens if you connect the load $R_L$ to your circuit? Is loading noticeable? Explain!

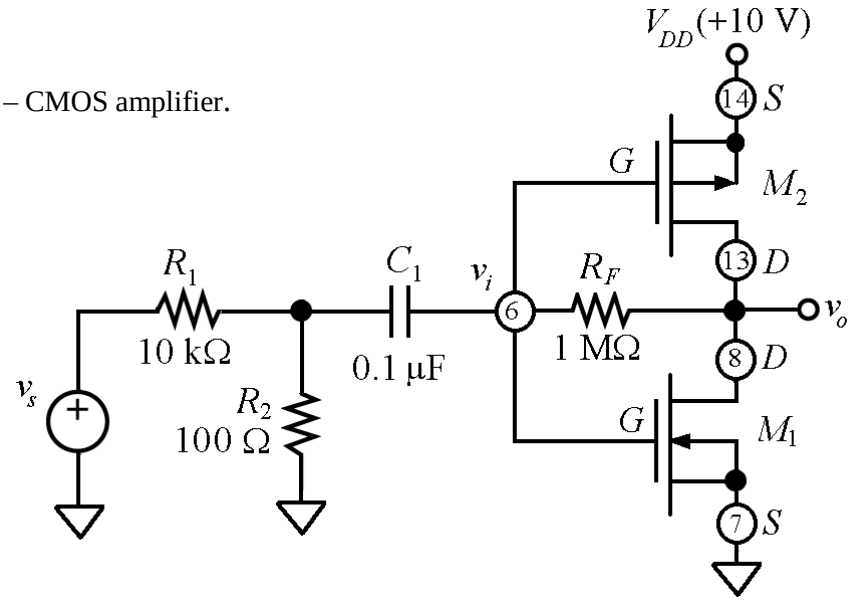
**CMS14:** Simulate the circuit of Fig. 16 via PSpice (DC as well as AC analysis), compare with predicted and measured values, and account for any possible discrepancies.

## CMOS Amplifier:

A widely used MOSFET amplifier configuration is the *complementary MOS* (CMOS) cell of Fig. 17, consisting of an *n*MOSFET and a *p*MOSFET with the *gates* tied together to form the *input* node, and the *drains* tied together to form the *output* node. Biasing is accomplished by a plain feedback resistance $R_F$, which can be made relatively large as the gate terminals draw zero current. Using the MOSFETs' large signal models, one can prove that with this resistor in place, the output and input nodes will automatically bias at the common DC value $V_O = V_I = V_{BIAS}$, where

$$V_{BIAS} = \frac{V_{tn} + \sqrt{k_p/k_n}\,(V_{DD} - |V_{tp}|)}{1+\sqrt{k_p/k_n}} \tag{21}$$

**Fig. 17** – CMOS amplifier.




Moreover, using the small-signal models, one can prove that the *ac gain* around this bias point is

$$A_v = \frac{v_o}{v_i} = \frac{-(g_{mn} + g_{mp} - 1/R_F) \times (r_{on} // r_{op})}{1 + (r_{on} // r_{op})/R_F} \tag{22}$$

where $g_{mn}$, $g_{mp}$, $r_{on}$, and $r_{op}$ are calculated via Eq. (14). To find $I_D$, we use Eq. (9) with $v_{GS} = V_I$.

As you assemble (with power off!) the circuit of Fig. 17, keep leads short and bypass the power supply with the usual 0.1-μF capacitor. Anticipating a relatively high gain, we need to keep the input $v_i$ suitably small, so we interpose the voltage divider $R_1$ and $R_2$ between the input source and the amplifier to suitably scale down the source. With the resistance values shown, we have $v_i \cong v_s/100$.

**C15:** Using the MOSFET parameter values found experimentally, predict the values of $V_{BIAS}$, $I_D$, and $A_v$ for the CMOS amplifier of Fig. 17.

**M16:** Apply power to the circuit of Fig. 17, but without connecting the waveform generator yet, and use the DVM to measure the output DC voltage $V_O$. Next, connect the waveform generator, and set it for a 10-kHz, 0-V DC *sine-wave*. While monitoring $v_s$ with Ch. 1 and $v_o$ with Ch. 2 of the oscilloscope, adjust the waveform generator until that $v_o$ has a *peak-to-peak* amplitude of 2 V. Measure the corresponding *peak-to-peak* amplitude of $v_s$, find $v_i = v_s/100$, and finally determine the voltage gain $A_v = v_o/v_i$ of your amplifier.

**S17:** Simulate the circuit of Step M16 via PSpice (DC as well as AC analysis). For a realistic simulation you need to create a PSpice model both for your *n*MOSFET and *p*MOSFET samples, using the above-measured values of $k_n$, $V_{tn}$, and $\lambda_n$, as well as $k_p$, $V_{tp}$, and $\lambda_p$.

**C18:** Compare the *predicted* values of Step C15 with the *measured* ones of Step M16 and the *simulated* ones of Step S17. Account for possible discrepancies.