Hamid Mahmoodi

Professor

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EDUCATION

Purdue University, West Lafayette, IN

PhD in Electrical and Computer Engineering, Aug. 2005
Thesis: Low-Power, High-Performance, and Robust Circuit Design in Nanoscale CMOS
Advisor: Professor Kaushik Roy

University of Tehran, Tehran, Iran

M.S. in Electrical and Computer Engineering, Aug. 2000
Thesis: Low-Power Design of Digital Systems Based on Adiabatic Switching Principles
Advisor: Professor Ali Afzali-Kusha

Iran University of Science and Technology, Tehran, Iran

B.S. in Electrical Engineering, Aug. 1998

PROFESSIONAL EXPERIENCES

School of Engineering, San Francisco State University, San Francisco, CA

- Professor of Electrical and Computer Engineering, Aug. 2016-present
- Associate Professor of Electrical and Computer Engineering, Aug. 2011-Aug. 2016
- Assistant Professor of Electrical and Computer Engineering, Aug. 2005-Aug. 2011

NanoElectronics Research Laboratory, Purdue University, West Lafayette, IN

- Graduate Research Assistant, Feb. 2001-Augusbt 2005
- Supervisor: Professor Kaushik Roy
- Active PhD research on low-power and high-performance circuit design for nanoscale technologies (the research was mostly funded by SRC and DARPA), fabricated 5 chips, filed 5 patents, and published numerous conference and journal papers

IC Design Center, University of Tehran, Iran

- Graduate Research Assistant, Oct. 1999-Dec. 2000
- Supervisor: Professor Ali Afzali-Kusha
- Active M.S. Research on Low-Power Digital Design Based on Adiabatic Switching Principles, fabricated one chip and numerous published conference and journal papers

Electronic Research Center, Iran University of Science and Technology, Tehran, Iran

- Design engineer in Automation and Control Laboratory to design control systems using microcontrollers and Programmable Logic Controllers (PLCs), May 1998-Oct. 1999
- Translated (from English to Persian) and published a textbook on PLCs, entitled "Programmable Logic Controllers: Principles and Applications"
- Designed a microcontroller based digital control laboratory
- Designed a serial EPROM programmer and emulator

- Designed an educational system for the Z80 microprocessor

Advanced Electronic Research Center, Iran Electronic Industries Co., Tehran, Iran

- Research Engineer, Oct. 1998-Oct. 1999
- Research on Satellite Command and Data Handling Systems

AWARDS AND HONORS

- Co-recipient of Best Paper Award in the Two-Year College Division at the American Society for Engineering Education Annual Conference and Exposition, June 2017
- Co-recipient of Best Paper Award in the Minorities in Engineering Division at the American Society for Engineering Education Annual Conference and Exposition, June 2015
- Co-recipient of Best Diversity Paper Award at the American Society for Engineering Education Zone IV Conference, Apr. 2015
- Inventor Recognition Award by Semiconductor Research Corporation (SRC) for the U.S. patent application entitled "Apparatus and Methods for Determining Memory Device Faults", June 2009
- Inventor Recognition Award by Semiconductor Research Corporation (SRC) for the U.S. patent application entitled "Self-Repairing Technique in Nano-Scale SRAM to Reduce Parametric Failures", Mar. 2009
- 2006 IEEE Circuits and Systems Society VLSI Transactions Best Paper Award
- SRC Technical Excellence Award, an award given by the Semiconductor Research Corporation (SRC) to our research team at Purdue University lead by Prof. Kaushik Roy for excellent research contributions, Oct. 2005
- Inclusion of biography in the 60th diamond edition of "Who's Who in America", Oct. 2005
- Certificate of successful completion of essential teaching seminar for engineering faculty, Sep. 2005
- Competent Toastmaster Award by Toastmasters International for completion of the toastmasters international communication and leadership program, Feb. 2005
- Best paper award in IEEE International Conference on Computer Design, Oct. 2004
- National Award from Iran Ministry of Culture for the best translated book of the year in the field of computer engineering "Programmable Logic Controllers (PLC)", 2001
- Ranked 5th in the national graduate schools entrance examination in Electrical Engineering, Iran, July 1998
- Distinguished student in the field of Electronics Engineering in the academic year 1997-98, Iran University of Science and Technology, Feb. 1998
- 3rd place prize in the contest for "Scientific and Practical Student Projects", Iran University of Science and Technology, June 1997
- Distinguished student in the field of Electronics Engineering in the academic year 1996-97, Iran University of Science and Technology, Feb. 1997

PUBLICATIONS

Books and Book Chapters:

1. H. Mahmoodi, "Low-Power and Variation-Tolerant Memory Design", In: S. Bhunia and S. Mukhopadhyay, Low-Power Variation-Tolerant Design in Nanometer Silicon (ISBN: 978-1-4419-7418-1), Chapter 5, pp. 151-183, *Springer*, 2011
2. A. Jalali and H. Mahmoodi, "Programmable Logic Controllers: Principles and Applications", Tehran: Iran University of Science and Technology Press, 1999

(Translation: Awarded the best translated book of the year by Iran Ministry of Culture in 2001)

Published Journal Papers (Refereed):

1. S. Tabrizchi, A. Panahi, F. Sharifi, H. Mahmoodi, A.H. Badawy, "Energy-Efficient Ternary Multipliers Using CNT Transistors," MDPI journal of Electronics, DOI: 10.3390/electronics9040643, Mar. 2020
2. M.R. Taheri, F. Sharifi, M.A. Shafiabadi, H. Mahmoodi, and K. Navi, "Spin-Based Imprecise 4-2 Compressor for Energy-Efficient Multipliers," SPIN, World Scientific, Vol. 9, No. 3, DOI: 10.1142/S2010324719500115
3. R. Kuttappa, A. Balaji, V. Pano, B. Taskin, and H. Mahmoodi, "RotaSYN: Rotary Traveling Wave Oscillator SYNthesizer," accepted for *IEEE Transactions on Circuits and Systems I*
4. T. Winograd, G. Shenoy, H. Salmani, H. Mahmoodi, S. Rafatirad, and H. Homayoun, "Programmable Gates Using Hybrid CMOS-STT Design to Prevent IC Reverse Engineering," *ACM Transactions on Design Automation of Electronic Systems*, vol. 23, no. 6, Dec 2018
5. K. Mehrabi, B. Ebrahimi, R. Yarmand, A. Afzali-Kusha, and H. Mahmoodi, "Read Static Noise Margin Aging Model Considering SBD and BTI Effects for FinFET SRAMs," *Elsevier Microelectronics Reliability Journal*, DOI: 10.1016/j.microrel.2016.07.003, July 2016
6. R. Kuttappa, H. Homayoun, H. Salmani, and H. Mahmoodi, "Reliability Analysis of Spin Transfer Torque based Look up Tables under Process Variations and NBTI Aging" *Elsevier Microelectronics Reliability Journal*, DOI: 10.1016/j.microrel.2016.03.003, May 2016
7. B. Ebrahimi, A. Afzali-Kusha, H. Mahmoodi, "Robust FinFET SRAM Design based on Dynamic Back-Gate Voltage Adjustment," *Elsevier Microelectronics Reliability Journal*, DOI: 10.1016/j.microrel.2014.04.015, vol. 54, no. 11, Nov. 2014
8. F. Moradi, G. Panagopoulos, G. Karakonstantis, H. Farkhani, D. T. Wisland, J. K. Madsen, H. Mahmoodi, and K. Roy, "Multi-level Wordline Driver for Robust SRAM Design in Nano-scale CMOS Technology," *Elsevier Microelectronics Journal,* DOI:10.1016/j.mejo.2013.09.009, vol. 45, no. 1, pp. 23-34, Jan. 2014
9. H. Mahmoodi, S. Lakshmipuram, M. Arora, Y. Asgarieh, H. Homayoun, B. Lin, and D. Tullsen, "Resistive Computation: a Critique," *IEEE Computer Architecture Letters*, DOI: 10.1109/L-CA.2013.23, vol. 13, no. 2, pp. 89-92, Feb. 2014
10. F. Moradi, T. V. Cao, E. I. Vatajelu, A. Peiravi, H. Mahmoodi, and D. T. Wisland, "Domino Logic Designs for High-Performance and Leakage-Tolerant Applications," *Elsevier Integration, the VLSI Journal*, DOI:10.1016/j.vlsi.2012.04.005, vol. 46, no. 3, pp. 247-254, June 2013
11. B. Afzal, B. Ebrahimi, A. Afzali-Kusha, and H. Mahmoodi, "An Analytical Model for Read Static Noise Margin including Soft Oxide Breakdown, Negative and Positive Bias Temperature Instabilities," *Elsevier Microelectronics Reliability Journal*, DOI:10.1016/j.microrel.2013.01.009, vol. 53, no. 5, pp. 670-675, May 2013
12. B. Afzal, B. Ebrahimi, A. Afzali-Kusha, and H. Mahmoodi, "Modeling Read SNM Considering Both Soft Oxide Breakdown and Negative Bias Temperature Instability," *Elsevier Microelectronics Reliability Journal*, DOI:10.1016/j.microrel.2012.07.026, vol. 52, no. 12, pp. 2948-2954, Dec. 2012
13. M. Houshmand Kaffashian, R. Lotfi, K. Mafinezhadand, and H. Mahmoodi, "Impacts of NBTI/PBTI on Performance of Domino Logic Circuits with High-k Metal-Gate

Devices in Nanoscale CMOS," *Elsevier Microelectronics Reliability Journal*, DOI: 10.1016/j.microrel.2012.03.012, vol. 52, no. 8, pp. 1655-1659, Aug. 2012

14. M. Houshmand Kaffashian, R. Lotfi, K. Mafinezhadand, and H. Mahmoodi, "Impact of NBTI on Performance of Domino Logic Circuits in Nano-Scale CMOS," *Elsevier Microelectronics Journal*, DOI: 10.1016/j.mejo.2011.09.009, vol. 42, no. 12, pp. 1327-1334, Dec. 2011
15. F. Moradi, S. K. Gupta, G. Panagopoulos, D. T. Wisland, H. Mahmoodi, and K. Roy "Asymmetrically-Doped FinFETs for Low-Power Robust SRAMs," *IEEE Transactions on Electron Devices*, DOI: 10.1109/TED.2011.2169678, vol. 58, no. 12, pp. 4241 – 4249, Dec. 2011
16. M. Houshmand Kaffashian, R. Lotfi, K. Mafinezhadand, and H. Mahmoodi, "An Optimization Method for NBTI-Aware Design of Domino Logic Circuits in Nano-Scale CMOS," *IEICE Electronics Express*, vol. 8, no. 17, pp. 1406-1411, Aug. 2011
17. M. Cho, J. Schlessman, H. Mahmoodi, M. Wolf, and S. Mukhopadhyay, "PostSilicon Adaptation for Low-Power SRAM under Process Variation," *IEEE Design and Test of Computers*, DOI: 10.1109/MDT.2010.137, vol. 27, no. 6, pp. 26-35, Nov. 2010
18. S. Paul, H. Mahmoodi, and S. Bhunia, "Low-Overhead F_{max} Calibration at Multiple Operating Points Using Delay-Sensitive-Based Path Selection," *ACM Transactions on Design Automation of Electronic Systems*, DOI: 10.1145/1698759.1698769, vol. 15, no. 2, pp. , Feb. 2010
19. H. Mahmoodi, V. Tirumalashetty, M. Cooke, and K. Roy, "Ultra Low Power Clocking Scheme Using Energy Recovery and Clock Gating," *IEEE Transactions on Very Large Scale Integration Systems*, DOI: 10.1109/TVLSI.2008.2008453, vol. 17, no. 1, pp. 33-44, Jan 2009
20. Y. Wang, H. Mahmoodi, L-Y. Chiou, H. Choo, J. Park, W. Jeong, and K. Roy, "Energy-efficient Hardware Architecture and VLSI Implementation of a Polyphase Channelizer with Applications to Subband Adaptive Filtering," *Journal of Signal Processing Systems*, DOI: 10.1007/s11265-008-0323-2, Dec 2008
21. S. Bhunia, H. Mahmoodi, A. Raychowdhury, and K. Roy, "Arbitrary Two-Pattern Delay Testing Using A Low-Overhead Supply Gating," *Journal of Electronic Testing: Theory and Applications*, DOI: 10.1007/s10836-008-5072-4, June 2008
22. K. Kim, H. Mahmoodi, and K. Roy, "A Low-Power SRAM Using Bit-Line Charge-Recycling," *IEEE Journal of Solid-State Circuits*, DOI: 10.1109/JSSC.2007.914294, vol. 43, no. 2, pp. 446-458, Feb. 2008
23. S. Mukhopadhyay, H. Mahmoodi, and K. Roy, "Reduction of Parametric Failures in Sub-100-nm SRAM Array using Body Bias," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, DOI: 10.1109/TCAD.2007.906995, vol. 27, no. 1, pp. 174-183, Jan. 2008
24. A. Datta, A. Goel, T. Cakici, H. Mahmoodi, D. Lekshmanan, and K. Roy, "Modeling and Circuit Synthesis for Independently Controlled Double Gate FinFET Devices", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, DOI: 10.1109/TCAD.2007.896320, vol. 26, no. 11, pp. 1957-1966, Nov. 2007
25. S. Mukhopadhyay, K. Kim, H. Mahmoodi, and K. Roy, "Design of a Process Variation Tolerant Self-Repairing SRAM for Yield Enhancement in Nanoscaled CMOS," *IEEE Journal of Solid-State Circuits*, DOI: 10.1109/JSSC.2007.897161, vol. 42, no. 6, pp. 1370-1382, June 2007
26. N. Banerjee, A. Raychowdhury, K. Roy, S. Bhunia, and H. Mahmoodi, "A Novel Low-Overhead Operand Isolation Technique for Low-Power Datapath Synthesis," *IEEE Transactions on Very Large Scale Integration Systems*, DOI: 10.1109/TVLSI.2006.884054, vol. 14, no. 9, pp. 1034-1039, Sep. 2006

27. S. Mukhopadhyay, H. Mahmoodi, and K. Roy, "A Novel High Performance and Robust Sense Amplifier Using Independent Gate Control in Sub-50nm Double-Gate MOSFET," *IEEE Transactions on Very Large Scale Integration Systems*, DOI: 10.1109/TVLSI.2005.863743, vol. 14, no. 2, pp. 183-192, Feb. 2006
28. Q. Chen, H. Mahmoodi, S. Bhunia, and K. Roy, "Efficient Testing of SRAM with Optimized March Sequences and a Novel DFT Technique for Emerging Failures due to Process Variations," *IEEE Transactions on Very Large Scale Integration Systems*, DOI: 10.1109/TVLSI.2005.859565, vol. 13, no. 11, pp. 1286-1295, Nov. 2005
29. H. Mahmoodi, S. Mukhopadhyay, and K. Roy, "Estimation of Delay Variations Due to Random-Dopant Fluctuations in Nanoscale CMOS Circuits," *IEEE Journal of Solid-State Circuits*, DOI: 10.1109/JSSC.2005.852164, vol. 40, no. 9, pp. 1787-1796, Sep. 2005
30. S. Mukhopadhyay, H. Mahmoodi, and K. Roy, "Modeling of Failure Probability and Statistical Design of SRAM Array for Yield Enhancement in Nano-Scaled CMOS," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, DOI: 10.1109/TCAD.2005.852295, vol. 24, no. 12, pp. 1859-1880, Dec. 2005
31. S. Bhunia, H. Mahmoodi, D. Ghosh, S. Mukhopadhyay, and K. Roy, "Low-Power Scan Design Using First Level Supply Gating," *IEEE Transactions on Very Large Scale Integration Systems*, DOI: 10.1109/TVLSI.2004.842885, vol. 13, no. 3, pp. 384-395, Mar. 2005
32. A. Agrawal, B. Paul, H. Mahmoodi, A. Datta, and K. Roy, "A Process-Tolerant Cache Architecture for Improved Yield in Nanoscale Technologies," *IEEE Transactions on Very Large Scale Integration Systems*, DOI: 10.1109/TVLSI.2004.840407, vol. 13, no. 1, pp. 27-38, Jan. 2005 (**Best paper award**)
33. H. Mahmoodi and K. Roy, "Diode-Footed Domino: A Leakage-Tolerant High Fan-in Dynamic Circuit Design Style," *IEEE Transactions on Circuits and Systems I*, DOI: 10.1109/TCSI.2004.823665, vol. 51, no. 3, pp. 495–503, Mar. 2004
34. J. Park, W. Jeong, H. Mahmoodi, Y. Wang, H. Choo, and K. Roy "Computation Sharing Programmable FIR Filter for Low Power and High Performance Applications," *IEEE Journal of Solid-State Circuits*, DOI: 10.1109/JSSC.2003.821785, vol. 39, no. 2, pp. 348–357, Feb. 2004
35. K. Roy, S. Mukhopadhyay, and H. Mahmoodi, "Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Submicrometer CMOS Circuits," *Proceedings of the IEEE*, DOI: 10.1109/JPROC.2002.808156, vol. 91, no. 2, pp. 305-327, Feb. 2003
36. K. Roy, S. Mukhopadhyay, and H. Mahmoodi, "Leakage Current in Deep-Submicron CMOS Circuits," *Journal of Circuits, Systems, and Computers*, DOI: 10.1142/S021812660200063X, vol. 11, no. 6, pp. 575-600, Dec. 2002
37. H. Mahmoodi, A. Afzali-Kusha, and M. Nourani "An Adiabatic Carry-Look Ahead Adder with Efficient Supply Clock Generator," *IEE Proceedings on Circuits, Devices and Systems*, DOI: 10.1049/ip-cds:20010439, vol. 148, no. 5, pp. 229-234, Oct 2001

Published Conference Papers (Refereed):

38. G. Kolhe, H.M. Kamali, M. Naicker, T. D. Sheaves, H. Mahmoodi, S. Manoj, H. Homayoun, S. Rafatirad, A. Sasan, "Security and Complexity Analysis of LUT-Based Obfuscation: From Blueprint to Reality," IEEE International Conference on Computer Aided Design, 2019.
39. N. Karimian, F. Tehranipoor, M. M. Kermani, and H. Mahmoodi, "Deep RNN-Oriented Paradigm Shift through BOCANet: Broken Obfuscated Circuit Attack," accepted for *Great Lake Symposium on VLSI*, May 2019

40. M. Gee, A. Akash Lal, A. Hercules, T. Sheaves, A. G. Enriquez, C. Chen, H. Jiang, Z. Jiang, W. Pong, H. Shanasser, K.-S. Teh, X. Zhang, and H. Mahmoodi, "Research Experience for Community College Students: Design and Optimization of Non-Volatile Latch using Anti-Fuse Memory Technology" Proceedings of 2019 ASEE Pacific Southwest Section Conference, April 4-6, 2019
41. V. Delaplaine, R. Colin, P. Leung, D. Ceron, A. David, A. G. Enriquez, W. Pong, Z. Jiang, C. Chen, K.-S. Teh, H. Mahmoodi, H. Jiang, and X. Zhang, "Introducing Emerging Computer Engineering Research to Community College Students through a Summer Internship Project on Development of a Mobile Gesture Recognition System", Proceedings of 2019 ASEE Pacific Southwest Section Conference, April 4-6, 2019.
42. A. Bituin, K. Kyain, Y. Ordonez, A. Maxwell, W. L. Tang, A. Enriquez, N. Langhoff, W. Pong, C. Chen, K. S. Teh, X. Zhang, H. Mahmoodi, H. Jiang, Z. Jiang, "Engaging Community College Students in Cutting-Edge Research in Topology Optimization", Proceedings of 2019 ASEE Pacific Southwest Section Conference, April 4-6, 2019.
43. A. Carlson, K. Reyna, J. Rico Ruiz, M. Vieyra, A. G. Enriquez, N. Langhoff, Y. Xu, C. Chen, W. Pong, H. Shahnasser, Z. Jiang, H. Mahmoodi, H. Jiang, K.-S. Teh, and X. Zhang, "Integrating Collapse Simulation of Building Structures into Internship Experiences for Community College Students," Proceedings of 2019 ASEE Pacific Southwest Section Conference, April 4-6, 2019.
44. A. Attaran, T. D. Sheaves, P. Mugula, and H. Mahmoodi, "Static Design of Spin Transfer Torque Magnetic Look Up Tables for ASIC Designs," *Great Lake Symposium on VLSI*, pp. 507-510, May 2018
45. V. Miftakhov, C. D. Prato, S. Tornoe, K. Lim, A. Attaran, A. Enriquez, C. Chen, H. Jiang, Z. Jiang, W. Pong, H. Shahnasser, K. S. Teh, X. Zhang, and H. Mahmoodi, "Research Experience for Community College Students: Design and Optimization of Nan-Volatile Latch using Resistive Memory Technology," *American Society for Engineering Education Zone IV Conference*, Mar. 2018
46. R. Carroll, B. Carrozza, J. Lopez, Y. Ordonez, E. Sanchez, D. Kim, A. Lee, M. Lino, A. Enriquez, W. Pong, X. Zhang, H. Mahmoodi, Z. Jiang, C. Chen, H. Jiang, and K. S. Teh, "Learning Assistive Device Design Through the Creation of 3D Printed Children's Prosthetics with Augmented Grip Diversity," *American Society for Engineering Education Zone IV Conference*, Mar. 2018
47. C. Amaro, P. Silva, A. Davies, J. Marin, J. Caballero, A.G. Enriquez, J. Liang, C. Chen, W. Pong, H. Shahnasser, Z. Jiang, H. Mahmoodi, H. Jiang, K.S. Teh and X. Zhang, "Integrating Structural Engineering Research into Internship Experiences for Community College Students," *American Society for Engineering Education Zone IV Conference*, Mar. 2018
48. K. Chang-Kam, K. Abad, R. Colin, C. Tolentino, C. Malloy, A. David, A. G. Enriquez, W. Pong, Z. Jiang, C. Chen, K.S. Teh, H. Mahmoodi, H. Jiang, and X. Zhang, "Engaging Community College Students in Emerging Human-Machine Interfaces Research through Design and Implementation of a Mobile Application for Gesture Recognition", *American Society for Engineering Education Zone IV Conference*, Mar. 2018 (**Best diversity paper award**)
49. J. Mercurio, K. Yamada, A. Choi, A. Iqbal, J. I. Guzman, A. G. Enriquez, X. Zhang, W. Pong, Z. Jiang, C. Chen, K.S. Teh, H. Mahmoodi and H. Jiang, "Inspiring Community College Students in Electrical and Computer Engineering Research through Live Digit Recognition using NVidia's Jetson TX1", *American Society for Engineering Education Zone IV Conference*, Mar. 2018
50. R. Yedinak, O. Granados, V. Tran, M. Vieyra, A. Maxwell, A. Enriquez, W. Pong, C.

Chen, K. Siong Teh, X. Zhang, H. Mahmoodi, H. Jiang, Z. Jiang, "Engaging Community College Students in Civil Engineering Research of Structural Health Monitoring using Acoustic Sensors", *American Society for Engineering Education Zone IV Conference*, Mar. 2018

51. A.G. Enriquez, N. P. Langhoff, W.S. Pong, H. Mahmoodi, X. Zhang, C. Chen, K. S. Teh, Z. Jiang, "Developing a Summer Research Internship Program for Underrepresented Community College Engineering Students," *American Society for Engineering Education Annual Conference and Exposition*, June 2017 (**Best Paper Award in the Two-Year College Division**)
52. B. Leung, Y. T. Huang, F. Lorenzo, S. Rodriguez, J. Young, A. Attaran, A. Enriquez, C. Chen, Z. Jiang, W. Pong, H. Shahnasser, K. S. Teh, X. Zhang, and H. Mahmoodi, "Engaging Undergraduate Students in Research: Efficient Logic Design in Nano-Scale using Spin Transfer Torque Memory Technology," *American Society for Engineering Education Zone IV Conference*, Apr. 2017
53. J. Yan, J. Dalton, K. Chang-Kam, B. Doronila, V. Melara, C. Thomas, I. Donovan, K. Bholla, A. G. Enriquez, W. Pong, Z. Jiang, C. Chen, K.S. Teh, H. Mahmoodi, H. Jiang, K. Okada, and X. Zhang, "Engaging Community College Students in Computer Engineering through Design and Implementation of a Versatile Gesture Control Interface," *American Society for Engineering Education Zone IV Conference*, Apr. 2017
54. A. Furlanic, P. Thomas, P. Armas, R. Medina, J. Lok, A. Enriquez, W. Pong, C. Chen, K.S. Teh, Z. Zhang, H. Mahmoodi, and Z. Jiang, "Engaging Community College Students in Earthquake Engineering Research with Smart Wearable Devices," *American Society for Engineering Education Zone IV Conference*, Apr. 2017
55. T. Mitchell, S. Sharp, M. Carlson, J. Piccolotti, G. Ramirez, J. Caballero, A. Enriquez, W. Pong, C. Chen, Z. Jiang, H. Mahmoodi, X. Zhang, and K. Teh, "3D Printing of Short-Fiber Composites as an Effective Tool for Undergraduate Education in Composite Materials," *American Society for Engineering Education Zone IV Conference*, Apr. 2017
56. R. Shafiq, H. Homayoun, H. Mahmoodi, and H. Salmani, "The ATPG Attack for Reverse Engineering of Combinational Hybrid Custom-Programmable Circuits," *Government Microcircuit Applications and Critical Technology Conference*, Mar. 2017
57. A. Attaran, H. Salmani, H. Homayoun, and H. Mahmoodi, "Dynamic Single and Dual Rail Spin Transfer Torque Look Up Table with Enhanced Robustness under CMOS and MTJ Process Variations," IEEE International Conference on Computer Design, Oct. 2016
58. S. S. Nabavi Larimi, M. Kamal, A. Afzali-Kusha and H. Mahmoodi, "Power and Energy Reduction of Racetrack-based Caches by Exploiting Shared Shift Operations," *IEEE/IFIP International Conference on Very Large Scale Integration*, Sep. 2016
59. D. Almasi, H. Homayoun, H. Salmani, and H. Mahmoodi, "Comparative Analysis of Hybrid Magnetic Tunnel Junction and CMOS Logic Circuits" *IEEE International System-on-Chip Conference*, Sep. 2016
60. T. Winograd, H. Salmani, H. Mahmoodi, and H. Homayoun, "STT-CMOS Hybrid Designs for Reverse-engineering Prevention," IEEE Design Automation Conference, June 2016
61. R. Kuttappa, H. Homayoun, H. Salmani, and H. Mahmoodi, "Comparative Analysis of Robustness of Spin Transfer Torque based Look up Tables under Process Variations" IEEE International Symposium on Circuits and Systems, May 2016
62. J. Rodriguez Gudiel, T. Tariq, M. Gamarra, D. Alvarez, D. Almasi, A. G. Enriquez,

C. Chen, Z. Jiang, W. Pong, H. Shanasser, K.-S. Teh, X. Zhang, and H. Mahmoodi, "Engaging Undergraduate Students in Nano-Scale Spin-Electronics Research through Summer Internship," *American Society for Engineering Education Zone IV Conference*, Apr. 2016

63. T. Winograd, H. Salmani, H. Mahmoodi, and H. Homayoun, "Preventing Design Reverse Engineering with Reconfigurable Spin Transfer Torque LUT Gates," *IEEE International Symposium on Quality Electronics Design*, Mar. 2016
64. T. Winograd, H. Salmani, H. Mahmoodi, and H. Homayoun, "STT-CMOS Hybrid Designs for Reverse-engineering Prevention," *Government Microcircuit Applications and Critical Technology Conference*, Mar. 2016
65. H. Salmani, H. Mahmoodi, and H. Homayoun "Logical Vanishability for Counterfeit Prevention," SMTA/CALCE Counterfeit Electronic Parts and Electronic Supply Chain Symposium, June 2015
66. A.G. Enriquez, W.S. Pong, H. Shahnasser, H. Mahmoodi, C. Chen, X. Zhang, K. S. Teh, N. P. Rentsch, "Assessing the Impact of Research Experiences on the Success of Underrepresented Community College Engineering Students," *American Society for Engineering Education Annual Conference and Exposition*, June 2015 (**Best Paper Award in the Minorities in Engineering Division**)
67. R. Melgar, A. Nash, M. Sun, C. T. Yoc, M. Amir, C. Chen, A. G. Enriquez, H. Jiang, H. Mahmoodi, W. Pong, H. Shanasser, K.S. Teh, and X. Zhang, "Teaching Brain-Inspired Visual Signal Processing via Undergraduate Research Experience," *American Society for Engineering Education Zone IV Conference*, pp. 117-131, Apr. 2015
68. T. Martinez, A. Flores-Renteria, J. Flores, J. Chun, C. Chen, H. Ryan, W. Pong, N. Ozer, H. Shahnasser, H. Mahmoodi, A. G. Enriquez, A. Cheng, K. Teh, and X. Zhang, "Engaging Community College Students in Earthquake Engineering Research on Real-Time Hybrid Simulation," *American Society for Engineering Education Zone IV Conference*, pp. 38-46, Apr. 2015
69. M. Kinsler, C. McGill, G. Rodriguez, W. Berrios, J. Chow, A. Enriquez, P. Grams, X. Zhang, H. Mahmoodi, W. Pong, and K.S. Teh "3D Printing as an Enabling Platform for Cross-Disciplinary Undergraduate Engineering Education and Research," *American Society for Engineering Education Zone IV Conference*, pp. 417-429, Apr. 2015
70. N. Ettedgui, J. Cooney, B. LaBaer, E. Frimpong, G. Szeto, A. G. Enriquez, K.S. Teh, C. Chen, H. Mahmoodi, W. Pong, H. Shanasser, and X. Zhang, "Engaging Community College Students in Engineering Research through Design and Implementation of a Cyber-Physical System for Myoelectric-Controlled Robot Car," *American Society for Engineering Education Zone IV Conference*, pp. 394-404, Apr. 2015
71. A. Enriquez, N. Langhoff, W. Pong, N. Ozer, H. Shanasser, C. Chen, H. Mahmoodi, E. Cheng, K.S. Teh, and X. Zhang, "Expanding the Community College Engineering Educational Pipeline through Collaborative Partnerships," *American Society for Engineering Education Zone IV Conference*, pp. 381-393, Apr. 2015 (**Best diversity paper award**)
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GRANTS AND CONTRACTS

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3. Collaborative research grant ($1,200,000 total, SFSU share: $200,000), Project: Logical Vanishability through Hybrid STT LUT Technology to Prevent Reverse Engineering, Role: PI from SFSU, Funded by *Defense Advanced Research Project Agency (DARPA)*, July 2017- July 2019
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16. Charles Babbage University Grant ($26,500), Project: Curriculum Development and Research Based on Synopsys EDA tools at SFSU, Role: PI, funded by *Synopsys Inc.*, Jan. 2010
17. S-STEM: Scholarships in SCI, TECH, ENG, and MATH proposal ($598,840), Project: Scholarship for Success in Engineering Excellence, Role: Co-PI, funded by *National Science Foundation (NSF)*, April 2009
18. CIS User grant from Stanford Nanofabrication Facility ($5,000), Project: Non-Volatile memory on Flexible Substrate, Role: PI, Oct. 2008

19. Synopsys CAD Tools Training Session donation, ($5,400), Project: SFSU-Synopsys Collaboration, Role: PI, Jan-Apr. 2008
20. Synopsys CAD Tools license donation, ($3,000), Project: SFSU-Synopsys Collaboration, Role: PI, Sep. 2008
21. IBM 65nm CMOS Process Design Kit and chip fabrication donation ($50,000 estimated value), Project: Fault Tolerant Computing Architecture for Nano-Scale CMOS, Role: PI, April 2008
22. SFSU mini-grant ($5,000), Project: Low Power Design of Digital Systems Using Energy Recovery Clocking and Clock Gating, Role: PI, Nov. 2005

TEACHING & RESEARCH ADVISING EXPERIENCES

- Courses taught at San Francisco State University:

  ENGR 212: Introduction to Unix/Linus for Engineers, ENGR 356: Basic Computer Architecture, ENGR 357: Basic Digital Lab, ENGR 378: Digital System Design, ENGR 453: Digital IC Design, ENGR 478: Design with Microprocessors, ENGR 696/697: Engineering Design project, ENGR 699: Independent Study, ENGR 844: Embedded Systems, ENGR 848: Digital VLSI Design, ENGR 850: Digital Design Verification, ENGR 852: Advanced Digital Design, ENGR 856: Nano-Scale Circuits and Systems, ENGR895: Applied Research Project, ENGR 897: Research, ENGR 898: Thesis, ENGR 899: Special Study
- As committee chair, supervised more than 100 M.S. students who have landed jobs at companies (Intel, Synopsys, Broadcom, Qualcomm, Cisco, SanDisk, HP, Symantec) or entered PhD programs (University of Minnesota, University of California Irvine, Drexel University, University of California Santa Cruz, University of Tokyo)

PROFESSIONAL ACTIVITIES & MEMBERSHIPS

- Reviewing papers for the following journals and conferences:
  1. IEEE Transactions on Very Large Scale Integration Systems (TVLSI)
  2. IEEE Transactions on Computer Aided Design (TCAD)
  3. IEEE Transactions on Nanotechnology
  4. ACM Journal of Emerging Technologies in Computing Systems
  5. IEEE Transactions on Circuits and Systems I (TCAS)
  6. Journal of Electronic Testing: Theory and Applications
  7. Elsevier Integration VLSI Journal
  8. Elsevier Microelectronics Journal
  9. International Symposium on Quality Electronic Design (ISQED)
  10. International Symposium on Low Power Electronics and Design (ISLPED)
  11. IEEE International Symposium on Circuits and Systems (ISCAS)
  12. IEE Electronics Letters
  13. IEE Proceedings Circuits, Devices & Systems
- NSF Proposal Review:
  1. Reviewer for NSF Partnership for International Research and Education program, Jan. 2015
  2. Panelist to review proposals submitted for Major Research Instrumentation grants in the NSF Division of Electrical, communications and Cybersystems, April 2013
  3. Panelist to review proposals submitted for NSF Nanotechnology Undergraduate Education (NUE) in Engineering, June 2012
  4. Panelist to review proposals submitted for Major Research Instrumentation grants in the NSF Division of Electrical, communications and Cybersystems, March 2012

5. Panelist to review proposals submitted in the Division of Electrical, Communications and Cybersystems at NSF, May 2007

- Technical program committee member of *International Symposium on Quality Electronic Design*, 2006-2015
- Technical program committee member and co-chair of *Workshop on Civic Technology and Smart Cities*, 2015
- Technical program committee member of *International Symposium on Low Power Electronics and Design*, 2009 - 2013
- Local arrangement chair for hosting technical program committee meeting of *International Symposium on Low Power Electronics and Design*, 2011 and 2013
- Session Chair in *Interdisciplinary Engineering Design Education Conference*, Mar. 2013
- Session Chair in *Design Automation Conference*, June 2012
- Session Chair in *International Symposium on Quality Electronic Design*, Mar. 2012
- Session Chair in *International Symposium on Quality Electronic Design*, Mar. 2011
- Member of Curriculum Advisor Board of Synopsys University Program, 2010-present
- Member of the *Institute of Electrical and Electronics Engineers (IEEE)*, 2000- present
- Program Committee Member of *International Microelectronics Olympiad of Armenia*, 2010 - present
- Technical program committee member of *IEEE Custom Integrated Circuit Conference*, 2005-2008
- Executive committee member of IEEE San Francisco Section, 2007-2008