SFSU – ENGR 301 – ELECTRONICS LAB

LAB #3: BJT CHARACTERISTICS AND APPLICATIONS

Objective:
To characterize *bipolar junction transistors* (BJTs). To investigate basic BJT *amplifiers* and *current sources*. To compare *measured* and *simulated* BJT circuits.

Components:
1 × 2N2222 *npn* BJT, 1 × 2N3906 *pnp* BJT, 1 × 1N4733 5.1 V, 1 W Zener diode, 2 × 0.1 μF capacitors, 1 × 100 μF capacitor, 1 × 10 kΩ potentiometer, and resistors: 1 × 100 Ω, 2 × 1.0 kΩ, 4 × 10 kΩ, 1 × 100 kΩ, and 2 × 1 MΩ (all 5%, ¼ W).

Instrumentation:
A curve tracer, a bench power supply, a waveform generator (sine/triangle waves), a digital multi-meter, and a dual-trace oscilloscope.

PART I – THEORETICAL BACKGROUND

Figure 1 shows the circuit symbols for the *npn* and the *pnp* BJTs, along with the packages and pin designations of the two popular devices we are going to be using in this lab: the 2N2222 *npn* BJT and the 2N3906 *pnp* BJT. Note that the *current directions* and *voltage polarities* of one device are *opposite* to those of the other. Moreover, by KCL, we have $i_C + i_B = i_E$, for both transistors.

When a low-power *npn* BJT is biased in the *forward-active* (FA) *region*, defined by the conditions

$$v_{BE} = V_{BE(\text{on})} \cong 0.7 \text{ V} \tag{1a}$$

$$v_{CE} \geq V_{CE(\text{EOS})} \cong 0.2 \text{ V} \tag{1b}$$

its *collector* current i_C depends on the applied *base-emitter* voltage drop v_{BE} and the operating *collector-emitter* voltage v_{CE} as

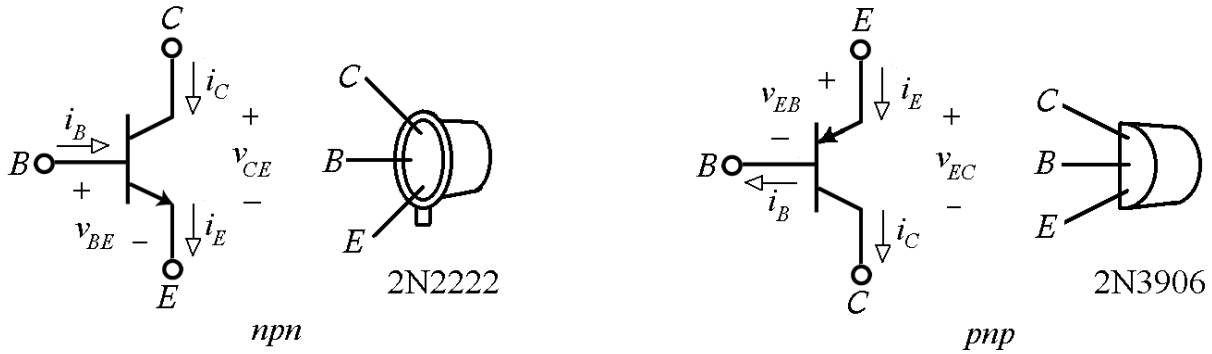


Fig. 1 – Circuit symbols, with current directions and voltage polarities of the *npn* and the *pnp* BJTs. Also shown are the packages of the popular 2N2222 *npn* BJT and 2N3906 *pnp* BJT.

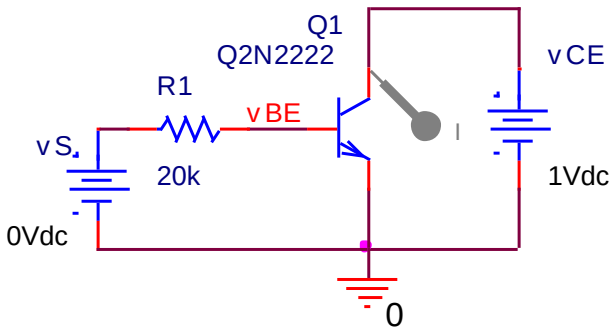


Fig.2 – PSpice circuit to display i_C versus v_{BE}.

$$i_C = I_s e^{v_{BE}/V_T}\left(1+\frac{v_{CE}}{V_A}\right) \qquad (2)$$

where

- I_s is a scale factor known as the *collector saturation current*
- V_T is a scale factor known as the *thermal voltage*
- V_A is yet another scale factor known as the *Early voltage*

At room temperature, $V_T \cong 26$ mV. Moreover, for a low-power BJT, the room-temperature value of I_s is typically on the order of fAs (1 FA = 10^{-15} A), and V_A is on the order of 10^2 V. The extrapolated value of i_C in the limit $v_{CE} \to 0$ is $i_C = I_s[\exp(v_{BE}/V_T)]$.

BJT circuits are readily simulated via PSpice. The PSpice library contains device models for a variety of popular BJTs, including the 2N2222 and 2N3906 of Fig. 1. Figure 2 shows a PSpice circuit to display the i_C versus v_{BE} characteristic of a 2N2222 BJT for a fixed value of v_{CE}. The result is shown in Fig. 3. The *slope* of the curve at a particular *operating point Q* is called the *transconductance*, and is denoted as g_m. Its units are A/V, or also 1/Ω. Slope depends on how far up we are on the curve, as

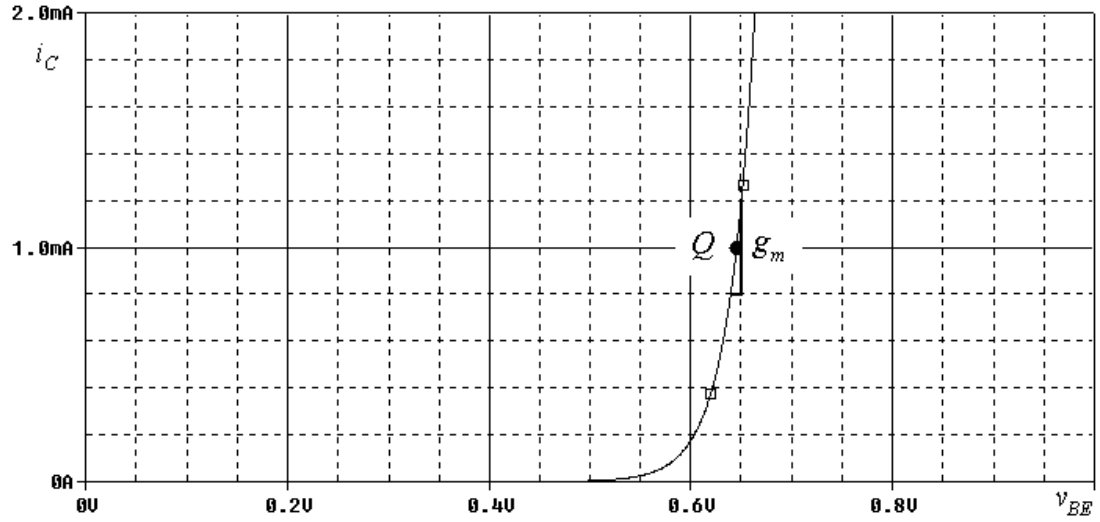


Fig. 3 – Plot of i_C versus v_{BE} for the BJT of Fig. 1.

$$g_m = \frac{I_C}{V_T} \tag{3}$$

To get a practical feel, remember that at I_C = 1 mA we have g_m = 1/26 = 38.5 mA/V = 1/(26 Ω).

Similar considerations hold for *pnp* BJTs, provided we *reverse* all *current directions* and *voltage polarities*. Thus, the forward-active conditions of Eq. (1) become, for a *pnp* BJT,

$$v_{EB} = V_{EB(\text{on})} \cong 0.7 \text{ V} \tag{4a}$$

$$v_{EC} \geq V_{EC(\text{EOS})} \cong 0.2 \text{ V} \tag{4b}$$

and Eq. (2) is rephrased as

$$i_C = I_s e^{v_{EB}/V_T}\left(1 + \frac{v_{EC}}{V_A}\right) \tag{5}$$

Likewise, the extrapolated value of i_C in the limit $v_{EC} \to 0$ is $i_C = I_s[\exp(v_{EB}/V_T)]$.

Another insightful way of illustrating BJT operation is by plotting i_C versus v_{CE} for different values of i_B. The PSpice circuit of Fig. 4 generates such a plot for incremental steps in i_B of 2 μA each. The resulting family of curves, shown in Fig. 5, reveals *three regions* of operation for the BJT:

- For $i_B = 0$, we get $i_C = 0$, indicating that the BJT is operating in the ***cutoff* (CO) *region***. In this region, the *base-emitter* (BE) *junction* and the *base-collector* (BC) *junction* are either reverse biased, or not sufficiently forward-biased to carry convincing currents, so both junctions act essentially as *open circuits*.
- For $i_B > 0$, the BJT is *on*. The region corresponding to $i_C > 0$ and $v_{CE} > V_{CE(\text{EOS})} \cong 0.2$ V is called the ***forward-active* (FA) *region***. Here, the *BE junction is forward biased* at $v_{BE} = V_{BE(\text{on})} \cong 0.7$ V, and the *BC junction is reverse biased*, or at most it is forward-biased at 0.7 – 0.2 = 0.5 V, which is *insufficient* to make it carry a convincing amount of forward current. In FA, the i_C versus v_{CE} curves are almost *horizontal*, indicating *current-source* behavior by the CE port there. If we project the FA curves to the left, they all converge to the *same point*, on the v_{CE} axis. This point is located at $-V_A$, the Early voltage appearing in Eq. (2).
- For $v_{CE} < V_{CE(\text{EOS})} \cong 0.2$ V, the curves turn almost *vertical*, indicating *voltage-source* behavior by the CE port there. The curves merge together at approximately $v_{CE} = V_{CE(\text{sat})} \cong 0.1$ V, and this region of operation is called the ***saturation region***. The borderline between the FA and the saturation regions is aptly called the *edge of saturation* (EOS).

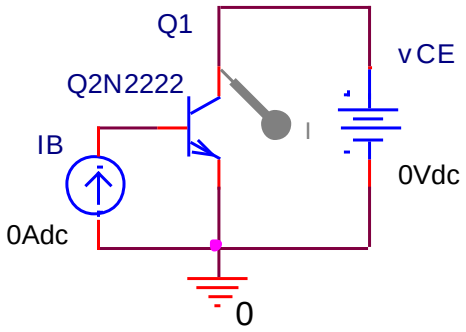


Fig. 4 – PSpice circuit to plot i_C versus v_{CE} for different values of i_B.

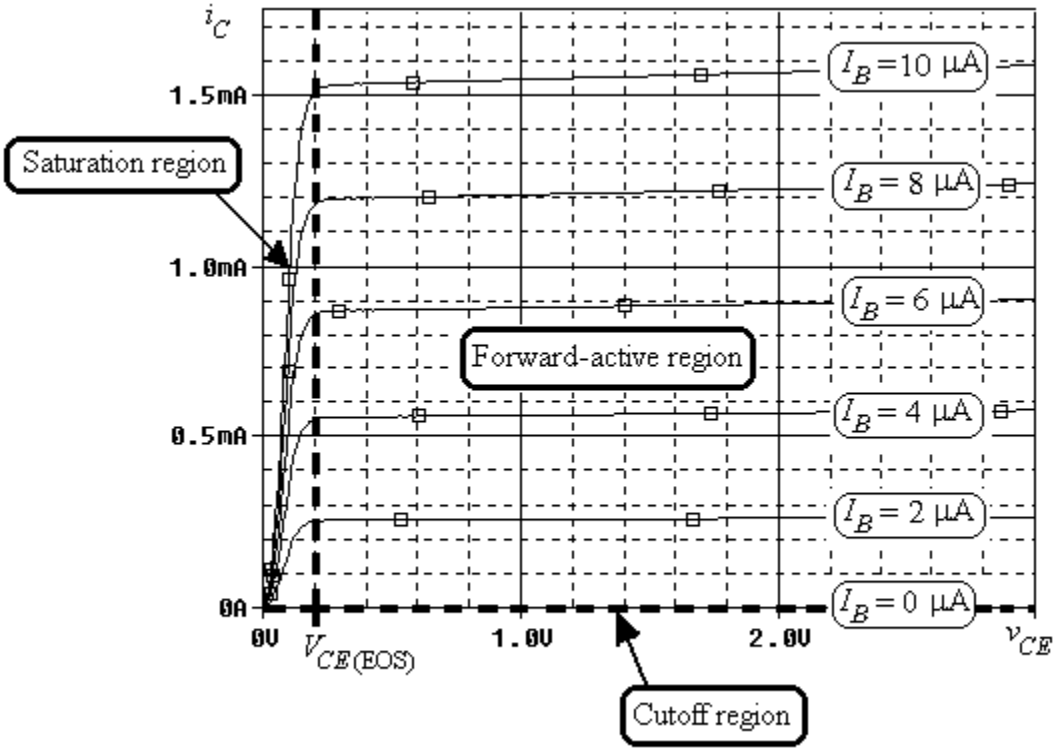


Fig. 5 – Illustrating the *three* regions of operation of an *npn* BJT.

Regardless of whether a BJT is of the *npn* or *pnp* type, its terminal currents in the *FA region* are related as

$$i_C = \alpha_F i_E = \beta_F i_B \qquad i_B = \frac{i_C}{\beta_F} = \frac{i_E}{\beta_F + 1} \qquad i_E = \frac{i_C}{\alpha_F} = (\beta_F + 1) i_B \tag{6}$$

where

$$\beta_F = \frac{\alpha_F}{1 - \alpha_F} \qquad \alpha_F = \frac{\beta_F}{\beta_F + 1} \tag{7}$$

Typically, α_F is very close to unity (such as $\alpha_F \cong 0.99$), and β_F, known as the *forward current gain*, is on the order of 10^2.

As we know, it is convenient to express a *total signal* such as the collector current i_C as the sum

$$i_C = I_C + i_c \tag{8}$$

where

- I_C is the *DC component*, also known as *large signal*
- i_c is the *AC component*, also known as *small signal*

We work with DC signals when dealing with transistor *biasing*, and we work with AC signals when dealing with *amplification*, to find AC *gain* as well as in *input* and *output resistances*.

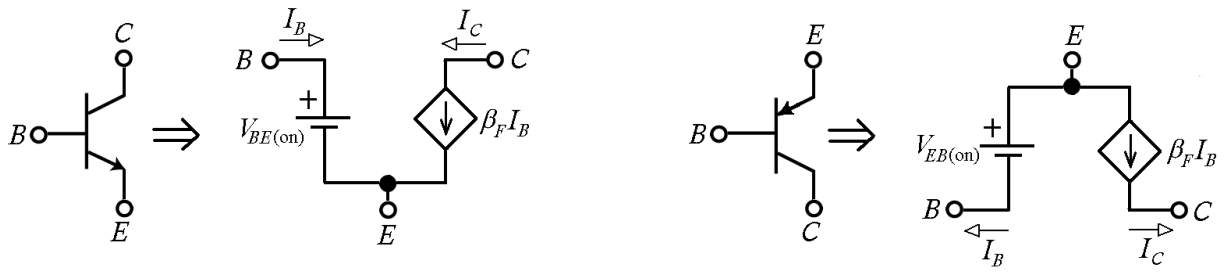


Fig. 6 – *Large-signal* BJT models in *the FA region*.

To signify how a BJT relates DC voltages and currents (upper-case symbols with upper-case subscripts) we use *large signal models*, while to signify how it relates AC voltages and currents (lower-case symbols with lower-case subscripts) we use the *small-signal model*.

Large-Signal BJT Models:

In each region of operation, a BJT admits a different large-signal model:

- In the *CO region*, a BJT draws only leakage currents, which for practical purposes are usually neglected. So, both junctions act essentially as *open circuits*.
- In the *FA region*, the BE port acts as a *battery* $V_{BE(on)} \cong 0.7$ V, while the CE port acts as a *dependent current source* $I_C = \beta_F I_B$. The two BJT models are shown in Fig. 6.
- In the *saturation region* the CE port too acts as a *battery*, namely, $V_{CE(sat)} \cong 0.1$ V, so the two BJT models are as in Fig. 7.

To gain additional insight into BJT operation, we use the PSpice circuit of Fig. 8 to sweep the BJT sequentially through each of the three operating regions. The resulting voltage transfer curves (VTCs), shown in Fig. 9, allow us to make the following observations:

- For $v_B < V_{BE(on)}$ the BJT is in cutoff, and $i_C = 0$. Consequently, $v_E = 0$ and $v_C = V_{CC} = 6$ V.
- As v_B approaches $V_{BE(on)}$, the BJT reaches the *edge of conduction* (EOC), and past that it enters the *FA region*, where it becomes fully conductive. Henceforth, we have $v_E = v_B - V_{BE(on)} \cong v_B - 0.7$ V, that is, the emitter will *follow* the base, albeit with an offset of about –0.7 V. Moreover, the circuit yields

$$v_C = V_{CC} - R_C i_C = V_{CC} - R_C \alpha_F i_E \cong V_{CC} - \alpha_F R_C \frac{v_B - V_{BE(on)}}{R_E} \cong \left(V_{CC} + \frac{R_C}{R_E} V_{BE(on)} \right) - \frac{R_C}{R_E} v_B$$

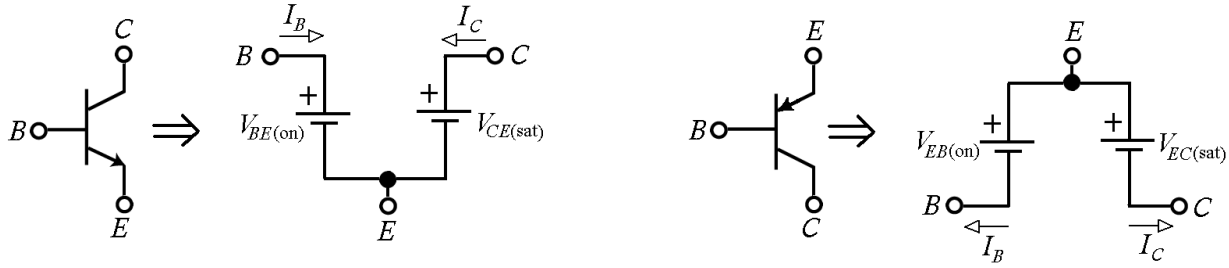


Fig. 7 – *Large-signal* BJT models in the *saturation region*.

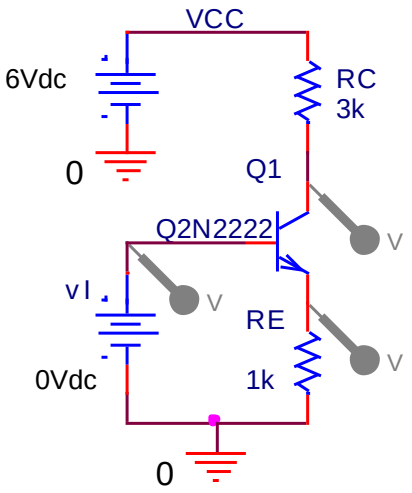


Fig. 8 – PSpice circuit to display the emitter and collector VTCs

Rewriting as $v_C \cong K + A_v v_B$, with K a suitable constant, we note that in the FA region the BJT *amplifies* v_B with the gain

$$A_v \cong -\frac{R_C}{R_E} \tag{8}$$

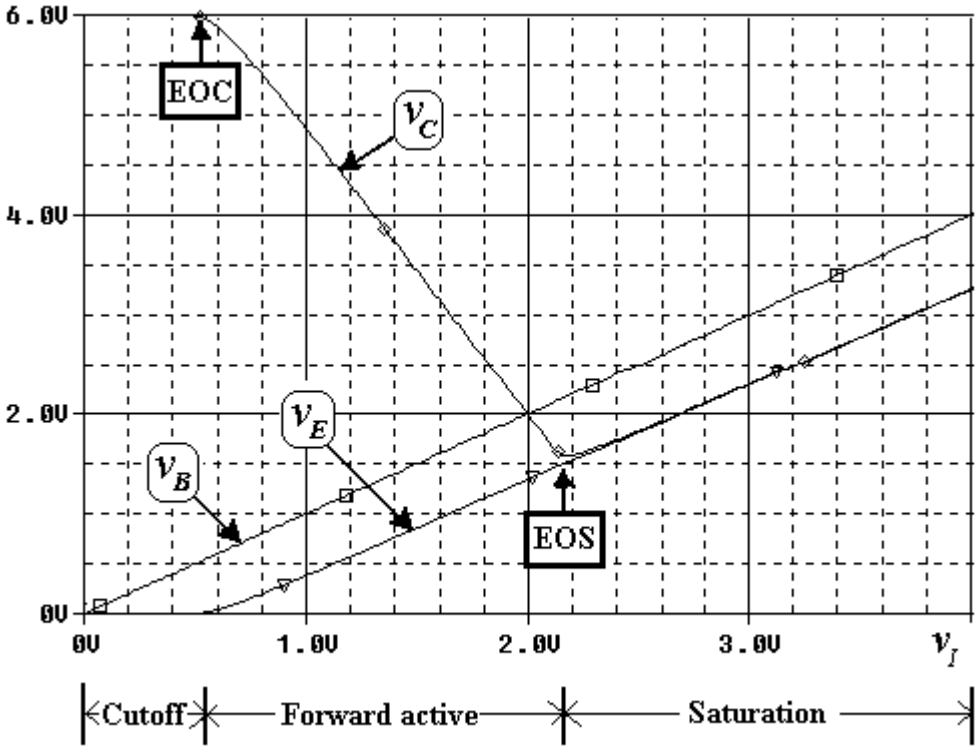


Fig. 9 – Voltage transfer curves for the circuit of Fig. 7.

or $A_v \cong -(3/1) = -3$ V/V. Figure 9 confirms this. Equation (8) forms the basis of the familiar **rule of thumb**: The gain of the circuit of Fig. 8 is approximately equal to the <u>*ratio of the collector resistance* R_C *to the emitter resistance* R_E</u>.

- As the BJT is pushed further into the FA region, v_C continues to drop at the rate of –3 V/V, until it comes within $V_{CE(EOS)}$ ($\cong$ 0.2 V) of v_E. As we know, this point is the *edge of saturation* (EOS).
- Past the EOS, the BJT is in *full saturation*, and v_C is now forced to ride about 0.1 V *above* v_E, which in turn we know to be riding about 0.7 V *below* v_B. Consequently, v_C will now be *rising* with v_B, albeit with an offset of –0.6 V.

Small-Signal BJT Model:

When used as an *amplifier*, a BJT is operated in the *FA region* where we model its way of relating voltage and current *variations* via the *small signal model*. Due to its exponential characteristic, the BJT is a highly nonlinear device. However, if we stipulate to keep its *signal variations sufficiently small* (hence the designation *small-signal*), then the model can be kept linear – albeit approximate. For BJTs, the small signal constraint is

$$v_{be} << 2V_T \cong 52 \text{ mV} \tag{10}$$

While the large-signal models are different for the two BJT types because they have *opposite* voltage polarities and current directions, the small-signal model is the *same* for the two devices because it involves only *variations*.

This common model is shown in Fig. 10, and is also called the π model because its elements are arranged in the form of an upside-down π. The dependent source can be considered as controlled either by v_{be} or by i_b, depending on which one is more convenient for AC analysis calculations. The parameters appearing in the small-signal model depend on the *bias current* I_C according to

$$g_m = \frac{I_C}{V_T} \qquad r_\pi = \beta_0 \frac{V_T}{I_C} \qquad r_o = \frac{V_A}{I_C} \tag{11}$$

where β_0 is the *small signal current gain*, usually taken to equal β_F. To develop a practical feel, we use the typical values $\beta_0 \cong 100$ and $V_A \cong 100$ V to find that, at $I_C = 1$ mA, a low-power BJT has typically

$$g_m = \frac{1}{26\ \Omega} \qquad r_\pi \cong 2.6\ \text{k}\Omega \qquad r_o \cong 100\ \text{k}\Omega$$

As we move from *E*, to *B*, to *C*, the resistance levels change from *small*, to *medium*, to *large*.

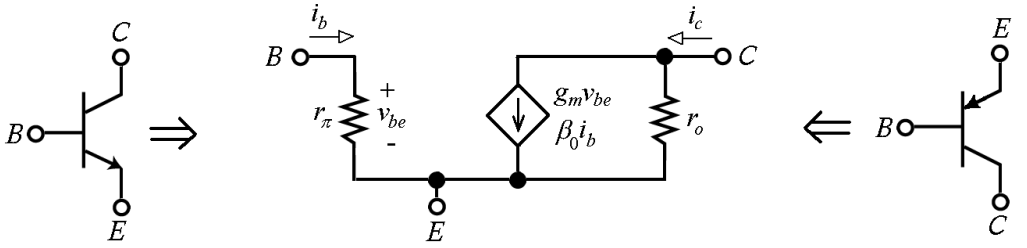


Fig. 10 – *Small-signal* BJT model (valid for $v_{be} << 2V_T \cong 52$ mV).

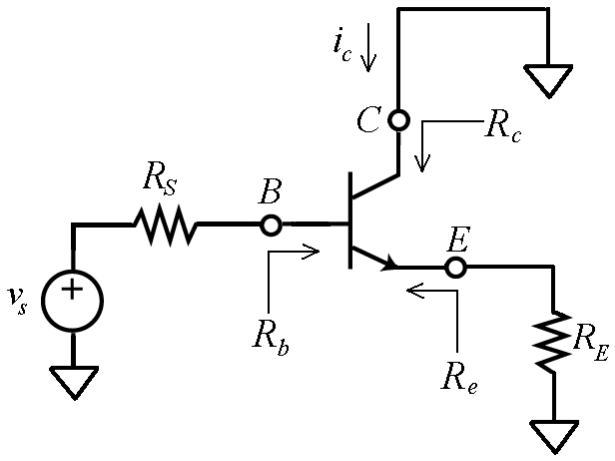


Fig. 11 – A generalized AC equivalent.

Figure 11 shows the *AC equivalent* of a generalized BJT circuit, whose properties are worth listing because they can be used to simplify the analysis of a variety of BJT amplifiers.

- The resistance seen looking into ***the base*** is

$$R_b = r_\pi + (\beta_0 + 1)R_E \tag{12}$$

indicating that the emitter resistance R_E, when reflected to the base, gets *multiplied* by (β_0 + 1). If $R_E = 0$, then $R_b = r_\pi$.

- The resistance seen looking into the ***emitter*** is

$$R_e = r_e + \frac{R_S}{\beta_0 + 1} \tag{13}$$

where $r_e = \alpha_F/g_m \cong 1/g_m$ is the resistance seen looking into the emitter in the limit $R_S \to 0$. As we know, at I_C = 1 mA we have r_e = 26 Ω. Equation (12) indicates that the base resistance R_S, when reflected to the emitter, gets *divided* by (β_0 + 1). Comparing Eqs. (12) and (13), we see that the resistance transformation by the BJT works both ways in reciprocal fashion, as in the case of the familiar transformer. In fact, the word *transistor* was coined to signify *trans*formation of a re*sistor*!

- The resistance seen looking into the ***collector*** is

$$R_c \cong r_o\left(1 + \frac{g_m R_E}{1 + (R_S + R_E)/r_\pi}\right) \tag{14a}$$

indicating that the presence of R_E effectively *raises* the collector resistance from r_o to the value of Eq. (14*a*). It often occurs that (R_S + R_E) << r_π, in which case we have

$$R_c \cong r_o(1 + g_m R_E) \tag{14b}$$

- The change in collector current i_c stemming from a small-signal change in the base voltage v_b is expressed as $i_c = G_m v_b$, where

$$G_m = \frac{g_m}{1 + g_m R_E} \qquad (15)$$

It is apparent that $G_m < g_m$, indicating that the presence of R_E *reduces* the BJT's transconductance. This loss is referred to as *degeneration*, and R_E is said to introduce *emitter degeneration*. In the limit $g_m R_E >> 1$, we get $G_m = 1/R_E$, that is, the transconductance no longer depends on the BJT, but is set *externally* by R_E. This offers important advantages, as we'll see in Step M13.

We conclude by illustrating the use of PSpice to simulate a *common-emitter* (CE) *amplifier*. As usual, you can simulate this circuit on your own by downloading its appropriate files from the Web. To this end, go to http://online.sfsu.edu/~sfranco/CoursesAndLabs/Labs/301Labs.html, and once there, click on **PSpice Examples**. Then, follow the instructions contained in the **Readme** file. The PSpice circuit is shown in Fig. 12*a*. After directing PSpice to perform the *Bias Point Analysis*, we obtain the labeled schematic of Fig. 12*b*. Moreover, after directing PSpice to perform a one-point *AC analysis* at f = 10 kHz, we find that the *small-signal gain* of the circuit is $A_v = v_o/v_i = -94.5$ V/V. You will find it quite instructive to confirm the above data (both bias and AC) via hand calculations!

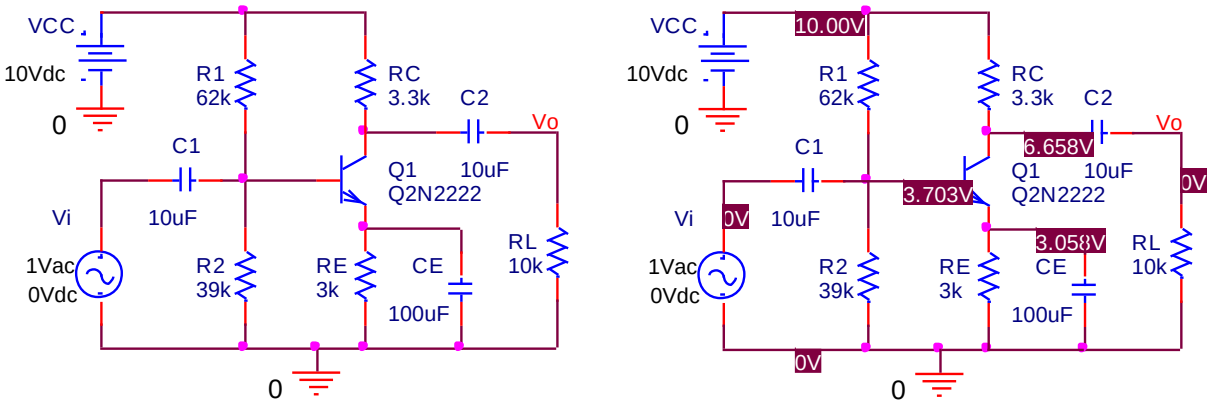


Fig. 12 – (*a*) PSpice CE amplifier and (*b*) its DC bias voltages

PART II – EXPERIMENTAL PART

The BJT data sheets give *typical* data, that is, data that were obtained by averaging over a large number of samples. The BJT models available in the PSpice library are based on typical data. Ddata sheets can readily be downloaded from the Web (for instance, go to http://www.google.com and search for "2N2222" and "2N3906" or variants thereof.) In this lab we shall characterize a *particular* BJT sample, and compare against the data sheets to assess how close our sample is to typical, as well as how realistic our PSpice simulations are.

Please refer to the Appendix for useful tips on how to construct proto-board circuits. In particular, always use 0.1-μF capacitors to *bypass your power supplies*, and always *turn off power before making any changes* in a circuit. Failure to do so may destroy your BJT, indicating that the measurements performed up to that point will have to be repeated on a different sample. Before proceeding, mark one of your 2N2222 BJTs (the other is a spare).

Henceforth, steps shall be identified as follows: **C** for calculations, **M** for measurements, and **S** for SPICE simulation. Moreover, each measured value must be expressed in the form $X \pm \Delta X$ (e.g. $\beta_F = 160 \pm 5$), where ΔX represents the estimated uncertainty of your measurement, something you have to figure out based on measurement concepts and techniques learned in Engr 206 and Engr 300.

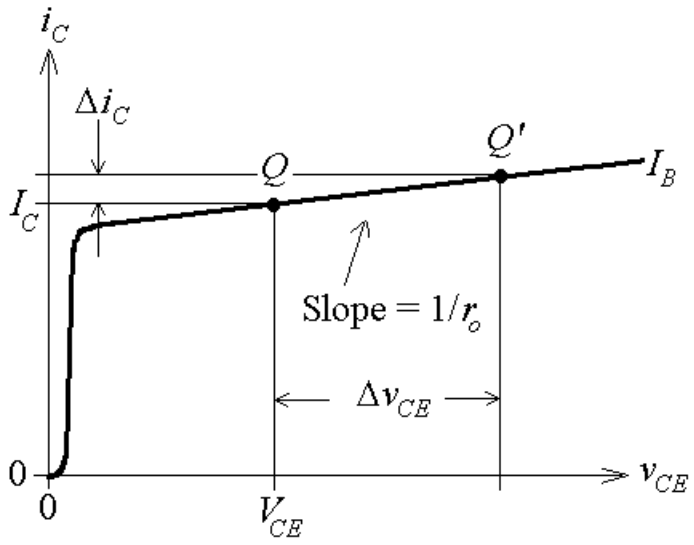


Fig. 13 – Graphical illustration for finding r_o and V_A.

Forward-Active Characteristics:

MC2: We now use the test circuit of Fig. 14 for a more accurate estimate of V_A. Thus, with power off, assemble the circuit, keeping leads short and bypassing the power-supply to ground via a 0.1-μF capacitor, as recommended in the Appendix. Then, while monitoring I_C with the *digital current meter* (DCM), apply power and adjust the potentiometer until $I_C = 0.5$ mA. This biases the BJT at the operating point $Q(I_C, V_{CE}) = (0.5 \text{ mA}, 5 \text{ V})$, as depicted in Fig. 13. Next, short out R_C with a wire (that is, close *SW*) so as to effect the change $\Delta V_{CE} = 5$ V and thus move the operating point from Q to Q' (see again Fig. 13). Record the corresponding change ΔI_C (this change is small, so use as many digits as your instrument will allow). Finally, compute

$$r_o = \Delta V_{CE}/\Delta I_C$$

$$V_A = r_o I_C - V_{CE}$$

where I_C = 0.5 mA and V_{CE} = 5 V.

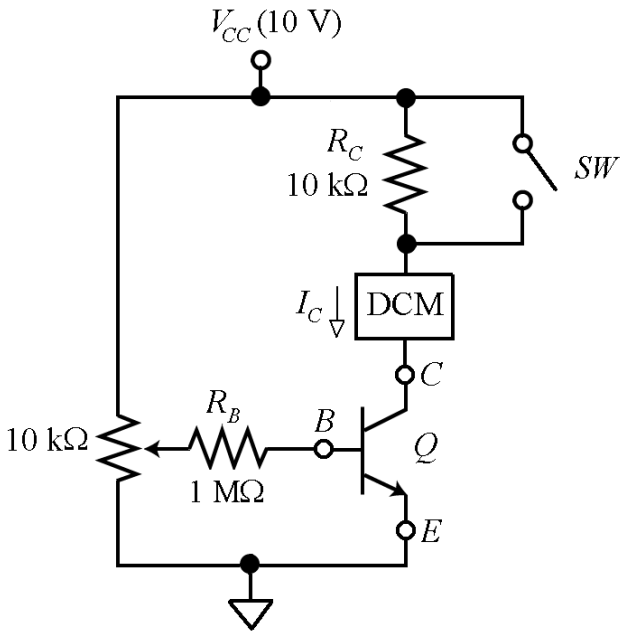
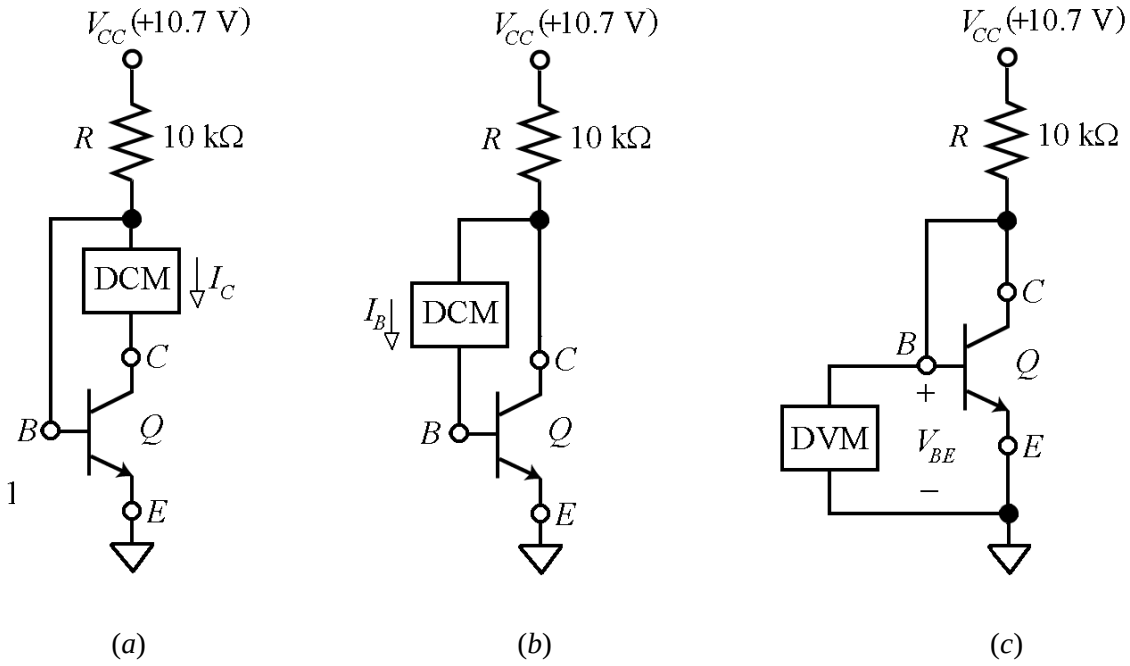


Fig. 14 – Test circuit to find r_o.and V_A.

MC3: We use the circuits of Fig. 15 for a more accurate estimate of β_F, as well as for finding I_s and V_T.



(*a*) (*b*) (*c*)

Fig. 15 – Test circuits to find β_F, I_s and V_T.

Thus, assemble the circuit of Fig. 15*a* and starting out with $V_{CC} \cong 10.7$ V, adjust V_{CC} for $I_C = 1.0$ mA. Next, turn power off, insert the DCM in series with the base as in Fig. 15*b*, reapply power without changing the setting for V_{CC}, and measure I_B. Finally, calculate

$$\beta_F = \frac{I_C}{I_B}$$

where $I_C = 1.0$ mA.

MC4: With power off, connect the *digital voltmeter* (DVM) in parallel with the base-emitter junction as in Fig. 15. Reapply power, and measure and record $V_{BE}(1\text{ mA})$. Next, turn power off and connect the BJT again as in Fig 15*a*, but with $R = 100$ kΩ. Reapply power and adjust V_{CC} for $I_C = 0.1$ mA. Then, with power off reconnect the BJT as in Fig. 15*c*, reapply power, and measure and record its new base-emitter voltage drop $V_{BE}(0.1\text{ mA})$.

Based on the above measurements, we can write two equations in the unknowns I_s and V_T,

$$1.0\text{ mA} = I_s e^{V_{BE}(1\text{ mA})/V_T}\left(1+\frac{V_{BE}(1\text{ mA})}{V_A}\right)$$

$$0.1\text{ mA} = I_s e^{V_{BE}(0.1\text{ mA})/V_T}\left(1+\frac{V_{BE}(0.1\text{ mA})}{V_A}\right)$$

where V_A is the Early voltage found in Step MC2, and V_{BE} (1.0 mA) and $V_{BE}(0.1\text{ mA})$ the *B-E* voltage drops just measured. Thus, substitute the given data and solve the two equations to obtain the experimental values of I_s and V_T. Are they typical?

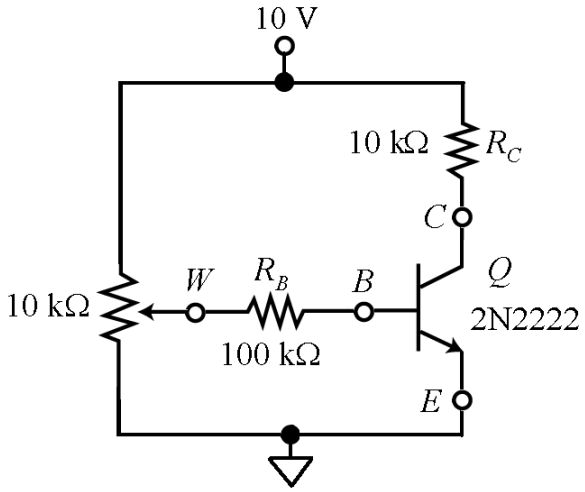


Fig. 16 – Test circuit for *saturation* measurements

Saturation-Region Characteristics:

MC5: To observe these characteristics we use the circuit of Fig. 16, which you assemble with power off. Next, apply power, and starting with the wiper voltage v_W at zero, gradually increase v_W while monitoring v_{CE} with the DVM. As you increase v_W, v_{CE} decreases until it finally saturates at $v_{CE} = V_{CE(\text{sat})}$. Record the values of V_W , V_{BE}, and V_{CE} at the point when the BJT *just begins* to saturate, known as the *edge-of-saturation* (EOS). Use the above data to calculate the ratio I_C/I_B at the EOS. How does this ratio compare with the value of β_F found earlier? Comment!

M6: Now increase v_W in the circuit of Fig. 16 all the way to 10 V while still monitoring v_{CE} with the DVM. Does v_{CE} change appreciably as the operating point is moved from the EOS to *deep saturation*? What is the value of the ratio I_C/I_B when v_W = 10 V? How does it compare with β_F? Justify the designation β_{forced} for the ratio I_C/I_B when operation is past the EOS.

Common-Emitter Amplifier:

With power off, assemble the circuit of Fig. 17 (implement R_{BIAS} with 2 × 10-kΩ resistors in series), keeping the leads short and bypassing the supplies with 0.1-μF capacitors to ground. By Eq. (10), the input v_i must be a *small signal* in order for the BJT to operate approximately linearly, so we interpose a voltage divider made up of R_1 and R_2 between the waveform generator and the BJT to suitably scale down the source signal. With the resistor values shown we have $v_i \cong v_s/100$.

C7: Assuming v_s has a DC value of 0 V in Fig. 17, use the large-signal BJT model to predict the DC voltages V_B, V_E, and V_C. Hence, predict the DC collector current I_C, as well as the value of the small-signal gain $A_v = v_o/v_i$, which in this case is

$$A_v = -g_m(r_o // R_C) \tag{16}$$

with g_m and r_o given in Eq. (11).

M8: Apply power to the circuit of Fig. 17, *but without connecting the waveform generator yet*, and use your DVM to measure the DC voltages V_B, V_C, and V_E. Next, connect the waveform generator, and while monitoring it with Ch.1 of the oscilloscope, adjust it so that v_s is a 10-kHz *sine-wave* with a *peak-to-peak* amplitude of 2 V and 0-V DC offset. Finally, use Ch. 2 to measure the *peak-to-peak* amplitude of v_o, and

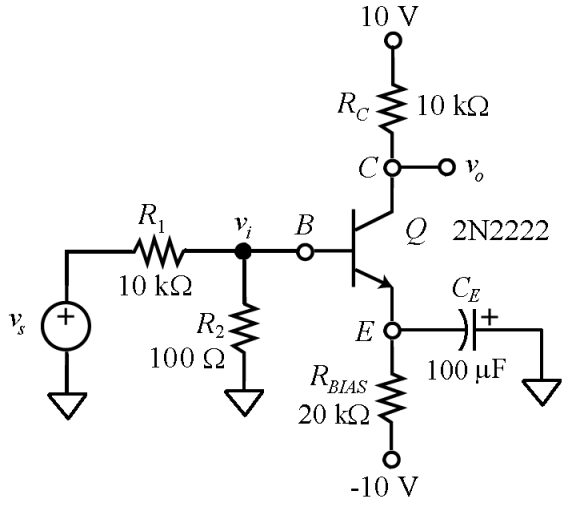


Fig. 17 – *Common-emitter* (CE) amplifier.

then find the gain $A_v = v_o/v_i$ of your amplifier, where $v_i = v_s/100$.

S9: Simulate the circuit of Step M8 via PSpice (DC as well as AC analysis). For a realistic simulation, you need to create a PSpice model for your *specific* BJT sample. To this end, when in PSpice, click your transistor to select it, then click **Edit → PSpice Model** and change the values of the parameters denoted as Is, Bf, and Vaf to the values found for I_s, β_F, and V_A in Steps MC2 through MC4.

C10: Compare the *predicted* values of Step C7 with the *measured* ones of Step M8 and the *simulated* ones of Step S9. Account for possible discrepancies.

M11: Returning to the circuit of Fig. 17, switch Ch. 2 back to the DC mode (make sure you know where your 0-V baseline is on the screen!), change the waveform generator from sine wave to *triangle wave*, and increase its amplitude first until v_o begins to *distort*, then until it *clips* both at the top and at the bottom (in case the generator's maximum amplitude is not large enough, you may have to remove R_2 from your circuit). What causes distortion to occur? What are the values of the upper and lower clipping voltages? Justify the two clippings in terms of the regions of operation of your BJT.

C12: The circuit of Fig. 18 is obtained from that of Fig. 17 by inserting the *emitter-degeneration* resistor R_E. Assuming v_s has a DC value of 0 V, find the collector current I_C, and predict the value of the small-signal gain $A_v = v_o/v_i$, which in this case is

$$A_v = -G_m(R_c // R_C) \tag{17}$$

where R_c and G_m are respectively given in Eqs. (14) and (15).

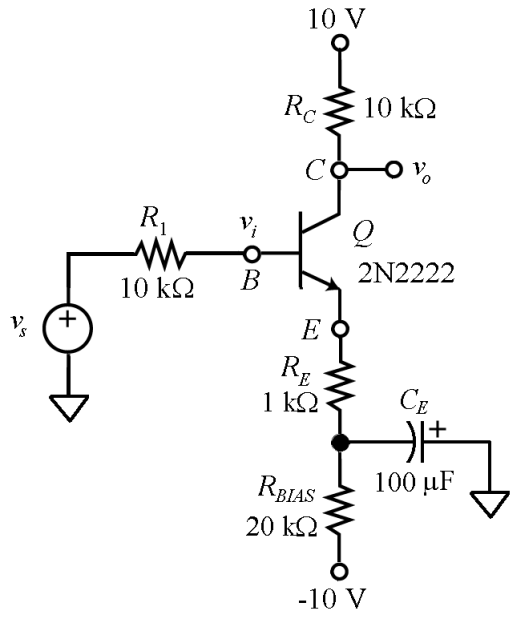


Fig. 18 – *Common-emitter* with *emitter degeneration* (CE-ED) amplifier.

M13: With power off, assemble the circuit of Fig. 18. Next, apply power, adjust the waveform generator so that v_i is now a 10-kHz sine-wave of 0.2-V *peak-to-peak* amplitude, and measure the gain $A_v = v_o/v_i$. How does it compare with the predicted value of Step C12? How does it compare with the rule-of-thumb value $A_v \cong -R_C/R_E$?

Common-Collector Amplifier:

C14: Assuming v_s has a DC value of 0 V in Fig. 19, use the large-signal model to find the DC collector current I_C. Hence, predict the value of the small-signal gain $A_v = v_o/v_s$, which in this case is

$$A_v = \frac{1}{1 + \dfrac{R_S + r_\pi}{(\beta_0 + 1)R_E}} \tag{18}$$

Also, predict the value of the output resistance R_o seen by the load, which in this case is $R_o = R_e // R_E$, with R_e given in Eq. (13).

M15: With power off, assemble the circuit of Fig. 19 (don't connect R_L yet.) Keep leads short, and mount the 0.1-μF power-supply bypass capacitors in *close proximity* to your circuit. Next, apply power, adjust the waveform generator so that v_s is a 10-kHz *sine-wave* with 0-V DC and a *peak* amplitude of 3 V, and measure the gain $A_v = v_o/v_s$. How does it compare with the predicted value of Step C14? What happens if you now connect the load R_L to your circuit? Is loading noticeable? Explain!

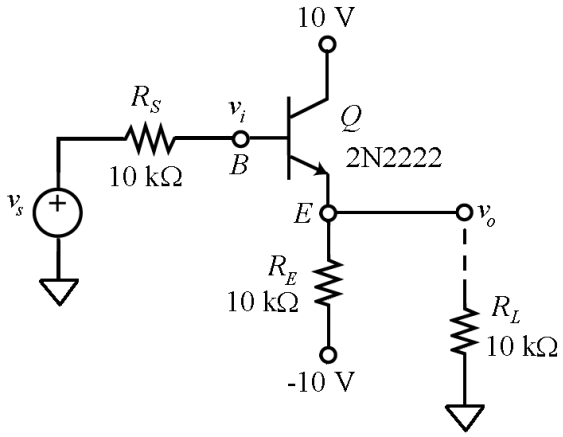


Fig. 19 – *Common Collector* (CC) amplifier.

Note: In this circuit v_s has a peak-to-peak amplitude of 6 V, hardly a small signal. Yet, we barely note any distortion, indicating that the BJT is still operating under small-signal conditions. Explain why!